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Title of Thesis – Titre de la thèse

"SWITCHED CAPACITOR OSCILLATORS"

Degree for which thesis was presented
Grade pour lequel cette thèse fut présentée

M. Sc.

Year this degree conferred
Année d'obtention de ce grade

FALL, 1985

University – Université

University of Alberta

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Switched Capacitor Oscillators

by

Ganesh Kothapalli

(C)

A THESIS

SUBMITTED TO THE FACULTY OF GRADUATE STUDIES AND RESEARCH

IN PARTIAL FULFILMENT OF THE REQUIREMENTS FOR THE DEGREE

OF Master of Science

DEPARTMENT OF ELECTRICAL ENGINEERING

EDMONTON, ALBERTA

FALL 1985

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To my Parents and Sister

ABSTRACT

The use of switched capacitor techniques has enabled the realization of precision analog circuitry suitable for realization in monolithic form. One of the most common circuits in analog electronic systems are oscillators. As large scale integrated techniques are being used to integrate systems, it is becoming increasingly important to develop techniques to efficiently implement these oscillators.

Salient features of the oscillators are obtained by exploiting the unique properties of SC circuits. The switched capacitor oscillators amplitude and frequency can be accurately controlled using a reference voltage and clock frequency respectively. The basic oscillator circuitry can be readily enhanced for the efficient generation of a variety of modulated signals.

It is observed from the investigation that SC oscillators, though they have higher levels of noise, are attractive due to their compatibility with CMOS technology. Other advantages and disadvantages are discussed.

The Wien oscillator and twin-T oscillator are chosen for experimental investigation. These oscillator circuits have been breadboarded with and without amplitude control circuits and aspects of their performance were confirmed.

A fast amplitude control method which restores initial conditions on a node (or nodes) is outlined. The oscillators amplitude control was achieved by variation of a reference

voltage. This method does not use a rectifier and thus the limitation of MOS technologies has been circumvented. MOS technology does not have floating diodes which are essential for most amplitude control methods.

The limiting type, AGC type and restoration types of amplitude control are compared. The restoration method of amplitude control is found to be the fastest among the three methods. The amplitude transients and the nonlinear distortions of the Wien and twin-T oscillators are studied. Though the twin-T oscillator has a longer amplitude transient of a few periods, the Wien oscillator amplitude control was achieved within one period. We were able to achieve total harmonic distortions of 0.2% in both the oscillators with the restoration method of amplitude control. The stability of the oscillators' amplitude was also verified by varying the power supply voltage over a wide range.

ACKNOWLEDGEMENTS

The author wishes to extend his sincere thanks to

- his supervisor Prof. I.M. Filanovsky for all the help, encouragement and guidance during the course of this work
- the Department of Electrical Engineering for providing the opportunity and financial assistance
- Prof. K.A. Stromsmoe for providing computing funds for production of this thesis
- Mr. G.J. Fortier for reading the manuscript
- his friends M. Parameswaran and G.J. Fortier for thier constructive suggestions

The author also wishes to express his indebtedness to his parents and family members, and to all his teachers for their invaluable contributions.

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LIST OF SYMBOLS

A	gain
BDI	Bilinear Discrete Integrator
Cr,CR,C_1,C_2..	Switched Capacitors
C_{mx}	maximum capacitance
exp	exponent
fc	clock frequency
fo	oscillation frequency
fs	signal frequency
k,K	constants
LDI	Lossless Discrete Integrator
N	nonlinearity, nonlinear amplifier
$\dot{r},\dot{\theta}$	polar coordinates (amplitude and phase respectively)
R,R_1,R_2..	Resistors
Req	Switched Capacitor Resistor equivalent
Roff	switch "off" resistance
Ron	switch 'on' resistance
SC	Switched Capacitor
SCO	Switched Capacitor Oscillator
SD	Sequence Discriminator
t,T	time
tp	clock period
THD	Total Harmonic Distortion
v,V,V_1,V_2..	voltages
Vg	gate voltage
Vi,Vin	input voltages

V_o, V_{out}	output voltages
V_{mx}	maximum voltage
V_p	peak voltage
V_r, V_{ref}, V_{Ref}	reference voltage
V_{th}	threshold voltage of MOS switches
w	angular frequency($=2\pi f$)
$x, y, \dot{x}, \dot{y}$	state variables
Y, Y_1, Y_2	admittance
z	z-transform
ϕ_1, ϕ_2	clock signals

1. INTRODUCTION

Switched capacitor circuits are sampled-data analog systems, and as such they occupy an intermediate position between fully analog (continuous-time/continuous-amplitude)and fully digital (discrete-time/discrete-amplitude) systems . In analog signal processing, especially filtering applications, they have so far offered several advantages over fully analog circuits. While the latter have up to now been fabricated mostly in discrete or hybrid forms, SC circuits are realized as integrated circuits, and hence are compact, reliable, and (for large-volume applications) inexpensive. Their frequency responses are controlled by clock signals; hence these circuits can readily be synchronized, multiplexed, and programmed[19]. Due to their sampled-data character, however, SC circuits must usually be preceded and/or followed by fully analog filters.

Oscillators play an important role in electronics. A laboratory in any area of science uses electronic instruments, particularly oscillators, to study the phenomena under investigation. Although not used themselves to measure electrical quantities , instruments that generate voltage waveforms of various frequencies and amplitudes are often useful for testing equipment, as well as for incorporation into various experiment systems. Sinusoidal waveform is fundamental, and units that produce this form as output have long been available. Some sort of oscillating circuit is involved, and the sine-wave generator is

therefore frequently referred to as an oscillator. A given circuit is usually limited in the range of frequencies over which it will operate; therefore, a given oscillator is usually an audio oscillator (frequency range about 1 hertz to <100 kilohertz), or a radio frequency oscillator (frequency range about 100 kilohertz to 100 megahertz).

Before we discuss the SC oscillators which are best suited for MOS technology, a few sentences about the RC oscillators realization in different integrated technologies (hybrid and completely integrated) is appropriate.

Hybrid integrated circuit technology, i.e., the combination of film resistors and capacitors with silicon integrated active devices, is applied to the design of integrated linear active networks. The passive components may be thick, or thin film, although in general, performance is found to be superior [46] with the latter type. Incidentally, the analytical simplifications resulting from the condition of closely tracking resistor and capacitor values will also be more accurate with thin-film implementation. It is observed that certain types of networks are more suited to the characteristics of this technology than others. One criterion of quality, or figure-of-merit, for the networks described can be seen to be preferable to another, depending on the technology for which the networks are intended. On these grounds it can be deduced that SC oscillators are more suitable for MOS realization. For example, the methods described in this

dissertation for design of SC oscillators and amplitude regulation do not require diodes and large capacitors,thus making them suitable for MOS realization. Moreover, the primary importance of analog circuits in future VLSI systems is expected to be in the area of interface circuits. These circuits connect the "real world" of analog, continuous time signals with the digital world of sampled (discrete-time) digitally-encoded signals. The desirability of a close relationship between these analog functions and digital circuits provides a strong impetus towards the use of a VLSI technology in which analog and digital circuit functions may be realized compatibly on the same circuit chip. The circuits investigated in this dissertation were breadboarded keeping in mind MOS realizations.

Thus far we can justify the choice of MOS technology for implementing SC oscillators. It is well established [19] that MOS technology is the desirable basis for the most complex circuits, thus traditional bipolar transistor integrated circuit and hybrid circuit approaches are not appropriate for SC realizations. The hybrid and bipolar transistor integrated circuits may still be attractive to applications where gain and noise parameter requirements are stringent.

In MOS technology, the high density of circuit elements makes it possible to implement complex functions, analog as well as digital, in modest chip areas. For example, an MOS operational amplifier, which is the active device for SC

oscillators, requires only 1/2 to 1/3 the die area of an operational amplifier in bipolar transistor technology. Also important is the capability to store and nondestructively sense signals on capacitors. Another important feature is the accuracy and stability of the MOS capacitor, which is the natural element for precision voltage and charge dividers in MOS technology.

1.1 Oscillators

Oscillator circuits differ in topology and complexity. Some can be realized using only one amplifier block with two RC sections while others may require either more RC sections, more amplifiers or both. With each of these circuits there is a minimum value of amplifier gain which is required to start the oscillation, and this gain condition may differ from one circuit type to another. This means that for a given amplifier, or amplifiers with similar characteristics, oscillators with different characteristics and limits may be realized since the frequency of oscillation is related to the passive circuit around it.

In order to simplify the study of oscillators it is convenient to classify them according to their common properties. It is from this kind of classification that one may easily choose a circuit to suit a certain application given the design and fabrication constraints. A convenient class of oscillators was chosen, and this dissertation outlines the basic theory of oscillation as applied to a

specific class, Switched Capacitor Oscillators derived from filter sections.

One way of studying SC oscillators is by examining the effect of the frequency determining sections(elements) together with the gain elements on the feedback signal. Thus simple oscillator circuits fall into two groups: the group of zero phase shift or Wien-type oscillators, and that of 180° phase shift or single-loop oscillators. The zero phase shift class of oscillators normally has a shunt SC network and a series SC network which provide phase cancellation. Other types of SC networks may be used to obtain the necessary zero phase shift, but these networks are more complex and uneconomical to fabricate in integrated form since they have more than two tuning capacitors.

From a circuit theory point of view, oscillators and active filters are quite related. In fact oscillators may be defined as conditionally stable active filters whose poles are adjusted to lie on the jw axis at $s=jw_o$ and whose inputs are grounded. It is therefore common practice to derive the properties of an oscillator from a study of the corresponding filter.

The characteristic equation (the denominator of a transfer function of an active filter equated to zero) may be divided into two parts, the "active portion" which is dependent on the amplifier gains and the "passive portion" which does not contain gain terms. The passive portion of the characteristic equation determines the type of filter in

terms of the order (first or second) of the decomposition.

The classification of oscillators follows closely that of active filters. Not all SC filters give rise to oscillators. A quick test for this is to examine the root locus and see whether it crosses the jw axis while gain is finite. If it does, then the filter may be used to realize an oscillator. Gain and sensitivity limitations for filters may be used to derive gain and sensitivity limitations for the corresponding oscillators. Second order oscillators in which the active portion of the characteristic equation is a function of s'only are attractive for integrated circuits. They have low gains and simple topologies.

Using the results of root locus analysis, a decision on the oscillator type most suited for a given task can be made. The choice of the practical circuit is influenced by the design constraints, the gain requirements of all possible circuits, parameter sensitivities and the tradeoffs involved. Usually, the design constraints for MOS realizations limit the number of convenient circuits to only a few and the choice is relatively simple. But, SC techniques allow most continuous oscillators to be implemented in MOS realization. Thus the gap between the wide choice of continuous oscillators and the limited choice of MOS realizable oscillators is narrowed. The limitation of continuous oscillators having large values of resistors, is circumvented by SC realizations.

Examples of Oscillators

In the following brief description of Wien and Twin-T oscillators is given.

(1) Wien-bridge oscillator:

In the connection of Fig.1.1a, a half-bridge built with identical RC elements applies positive feedback to the non-inverting input of an operational amplifier whilst a frequency-independent divider (RA,RB) provides a negative feedback path towards the inverting input.

An analysis of this circuit shows that the design should accomodate a gain of three, lest the circuit may not oscillate. The Wien-bridge oscillator circuit with the gain of the feedback amplifier adjusted to be less than three becomes a second-order bandpass active filter.

Partial s.c. oscillators:

Because all SC circuits require a clock that is an oscillator, one may wonder about circuits that use something to create the same thing. However to have possibility to change frequency, it is advantageous to realize the frequency determining elements using SC technique and the remaining circuitry using continuous elements.

Thus, the resistors R (in Fig.1.1a) are replaced by SC equivalents as shown in Fig.1.1b. The SC equivalent is comprised of a two-phase switch and a capacitor CR. As the capacitor CR is switched between two nodes at a clock frequency fc, an equivalent resistance of magnitude

Req = 1/fc.CR is simulated.

(2) Twin-T oscillator:

Another oscillator investigated is based on a notch network. This is shown in Fig.1.2 where oscillatory buildup is achieved with negative feedback through a mismatched twin-T network. In the vicinity of the resonant frequency, the phase shift around the mismatched feedback loop is 180°; consequently the originally negative feedback becomes positive.

It is shown in Chap.4 that a matched twin-T leads to a phase ambiguity at the resonant frequency. But, the required amount of mismatch is usually so small that even component tolerances may suffice to ensure it.

The switched capacitor equivalent of Fig.1.2a is shown in Fig.1.2b.

Because of the three energy storage elements, finding an amplitude control method with one period of amplitude transient is difficult. But the node voltage restoration method of amplitude regulation has only 2-3 periods of amplitude transient.

1.2 Amplitude control

A stable sine-wave oscillator with amplitude stabilization by conventional methods incorporates a controlled conductance or its equivalent. The D.C. control input to this conductance must have very small low frequency ripple or else an excessive distortion of the output waveform results. If this D.C. signal is derived from the usual half-wave rectifier an extremely large filter time

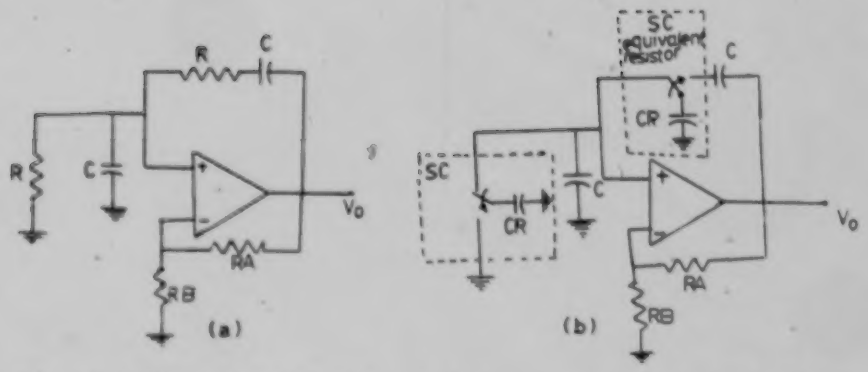


Fig. 1.1 Wien-bridge Oscillator (a) RC circuit (b) SC circuit.

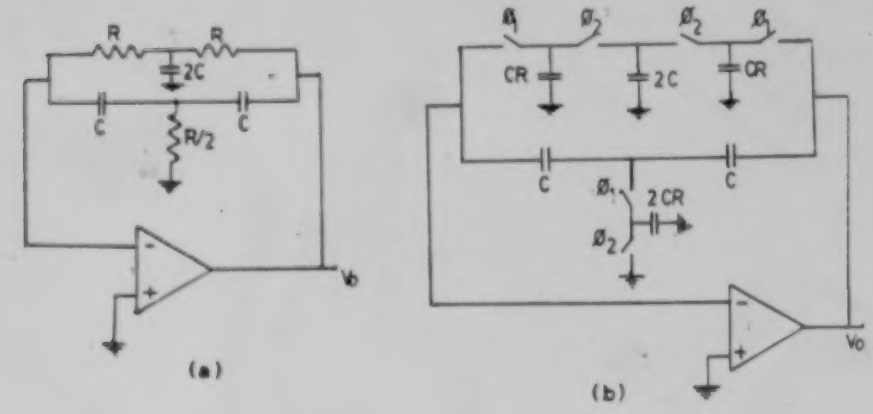


Fig.1.2 Twin-T Oscillator (a) RC circuit (b) SC circuit.

constant is required. The oscillator output level consequently settles very slowly if we try to change it. Moreover, the conventional amplitude control system of an oscillator effectively includes an integrator because the energy conserved in the oscillating system cannot disappear or increase instantly. As a result the amplitude control loop can be unstable and the oscillator has self modulation. Thus the first problem which arises in the design of the amplitude control system is to find a fast method for transforming a sinusoidal voltage into a D.C. voltage which is proportional to the amplitude. These methods have to use circuits which do not include any reactive or delay elements [59]. Further reduction of the output settling time depends on the realization of the controlled conductance. The current loading ability of these elements determines the available energy which we can pump into or out of the oscillating system. Consequently, the maximum speed of the amplitude settling depends on the current which can be built up in these voltage controlled conductances.

The block diagram for a typical amplitude control system (shown in Fig.1.3) will include an amplifier of gain K with a RC/SC two-port in the feedback path. The conductance control circuit may employ JFETS, multipliers, and other similar approaches. In the AGC type, amplitude control is facilitated by the use of a reference voltage.

AGC loops are used in many modern communication systems ranging from simple radio and mobile links to more complex

satellite systems. In most of these systems, however, the input signal level may vary rapidly and over a wide range of values. When this is the case linear AGC models are no longer helpful and a nonlinear problem has to be solved.

Where amplitude stability and distortion requirements are not very critical a simple limiting circuit may be adapted for oscillator amplitude stabilization. Usually the limiting type of stabilization does not provide means to vary the oscillation amplitude. In the limiting method, control circuits monitor the instantaneous value of the output signal of the oscillator and introduce a nonlinearity into the maintaining amplifier when the amplitude exceeds a certain value. Often the nonlinearity contained in the circuit is a saturation (compression) amplifier. A typical block diagram of limiting type amplitude stabilization is shown in Fig.1.4.

Since most methods of amplitude control use a floating diode in the control loop, the unavailability of a floating diode in MOS technology may be an inconvenience except when the restoration method is used. Complementary MOS technologies usually include process steps that can be used to form a parasitic transistor whose collector is tied to the substrate. The substrate is usually tied to one of the power supplies. As a result the floating diode is not available and the conventional circuits of amplitude control are unrealizable.

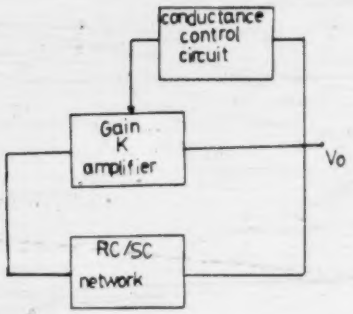


Fig. 1.3 AGC type amplitude control.

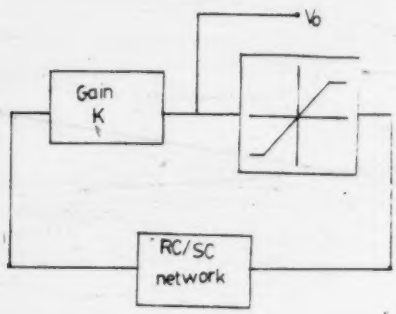


Fig. 1.4 Limiting type amplitude stabilization.

Node voltage restoration:

Two nodes of the oscillator, the synchronizing node "s" and the restoring node "r", are chosen for connection of the node voltage restoring circuit for fast amplitude regulation (Fig.1.5). When the synchronizing voltage becomes zero and the restoring voltage is positive (we assume that the phase shift between these two voltages is less than 180°) a control pulse is applied to the restoring node to establish initial conditions. The zero crossing of the synchronizing voltage can be identified by appropriate comparator. At this instant the control circuit interferes with the oscillator for a very short period of time. It closes momentarily a switch and the restoring voltage becomes instantly equal to Vref, the reference voltage. This procedure is repeated once in each oscillation period making it a fast amplitude control circuit besides other advantages as low distortion and high stability. The choice of the restoration node is determined by the lowest total harmonic distortion. In oscillators which contain two energy storing elements for instant Wien bridge oscillator, the new amplitude is achieved within one period of oscillation. Whereas in oscillators which contain three capacitors, establishing new amplitude is little longer.

Some aspects of oscillators and amplitude regulation circuits were not covered in this dissertation in detail. For instance, analysis methods, sensitivities, tolerances of components and temperature dependency. A thorough study

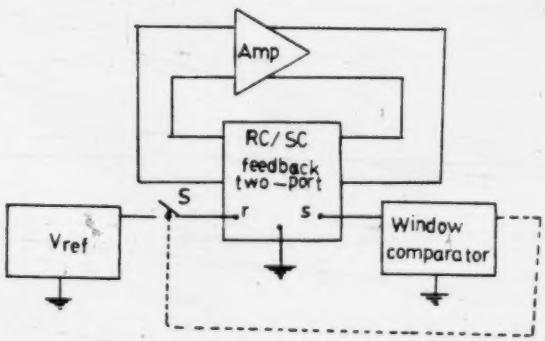


Fig.1.5 Amplitude control by node voltage restoration.

should also include the performance of oscillators with unequal duration of clock phases and multiphase clocking.

2. BASIC ELEMENTS OF SWITCHED CAPACITOR CIRCUITS

2.1 Principle of MOS Switched Capacitor Resistor

A simple but very fundamental feature of switched-capacitor circuits is the use of a capacitor and a number of analog switches to simulate the circuit behavior of a resistor, as shown in Fig.2.1. Assuming that the circuit nodes 1 and 2 are voltage sources with negligible impedance, the simulation of a resistor can be described as follows.

With the switch in the left-hand position, as shown in Fig.2.1, the capacitor C_1 is charged to the voltage V_1. Then the switch is thrown to the right, and the capacitor is discharged to the voltage V_2. For each cycle of the switch, a total unit charge Q_0 is transferred from one node to another, where

$$Q_0 = C_1\Delta V = C_1(V_1 - V_2) \qquad (2.1\text{-}1)$$

If the switch is operated at a clock frequency fc, this amount of charge transfer per switch cycle would correspond to an equivalent current flow Ieq, where

$$Ieq = Q_0 fc = C_1 fc(V_1 - V_2) \qquad (2.1\text{-}2)$$

In other words the switched capacitor C_1 behaves as a conveyor belt, delivering discrete packets of charge from one node of the circuit to another, where the total amount of charge delivered per unit of time (i.e., Ieq) is proportional to the size of the capacitor and the frequency of switching.

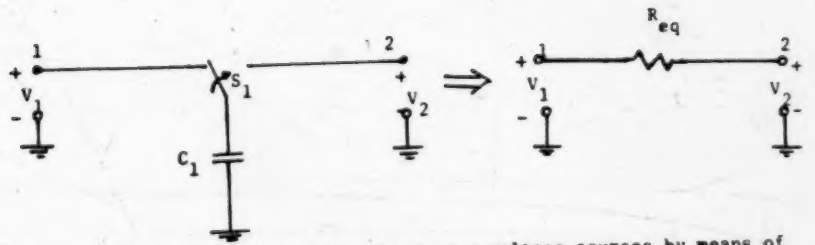


Fig. 2.1 Simulation of resistor across two voltage sources by means of a switched capacitor

$$Req = (V_1-V_2)/Ieq = 1/(C_1fc) \qquad (2.1\text{-}3)$$

It should be remembered that the Req given by eq.(2.1-3) can be used to replace a conventional resistor only under special conditions, where the two implicit assumptions used in its derivation are satisfied, namely,

1. The sampling frequency fc is much higher than the signal frequencies of interest.
2. The voltage V_1 and V_2 at nodes 1 and 2 are unaffected by switch closures (i.e., V_1 and V_2 are voltage sources with virtually zero impedance).

The first assumption stems from the sampled-data nature of the switched capacitor circuits. The second assumption is necessary to avoid the circuit transients and the instantaneous signal level changes due to switch closures. Both these assumptions can be satisfied by the proper choice of switch frequencies and circuit configuration.

For nonconstant values of V_1 and V_2 the effective resistance given by eq.(2.1-3) varies proportionally to the difference of the two voltages.

If an RC time constant is formed by combining the effective resistor Req of Eq.(2.1-3) with a discrete capacitor C_2, the resulting time constant teq would be

$$teq = ReqC_2 = C_2/(C_1fc) \qquad (2.1\text{-}4)$$

which is proportional to the capacitor ratio and inversely proportional to the clock frequency fc. Since monolithic capacitors are extremely stable, and their ratio can be very accurately controlled, one can now generate very accurate

time constants.

2.2 MOS transistor as an analog switch

MOS transistors make good analog switches for sampling, steering, or multiplexing analog signals. Fig.2.2 shows an idealized equivalent circuit of an MOS transistor as an analog switch. For illustrative purposes, an NMOS device is assumed.

When the gate voltage Vg is at or near ground, the device is off, and the source and drain terminals are isolated from each other by a nonconductive channel. When Vg is increased to a level such that Vg > Vth , a conductive channel is produced and a low-resistivity path is formed between the source and the drain. In actual operation, the MOSFET is a non ideal switch, having a number of parasitic capacitances associated with it, as shown in Figure.2.3.

The capacitances CGS, CGD, CSB, and CDB are the parasitic capacitances between the gate, source, drain, and body (i.e., substrate) regions of the device.

2.2.1 Effects of parasitic capacitances

In designing analog switches or selecting the device geometries and configurations for switches, the relative effects of the inherent device parasitics, primarily the four stray capacitances between gate, source, drain, and body, must be kept in mind. All of these capacitances increase with increasing device geometry and W/L ratio

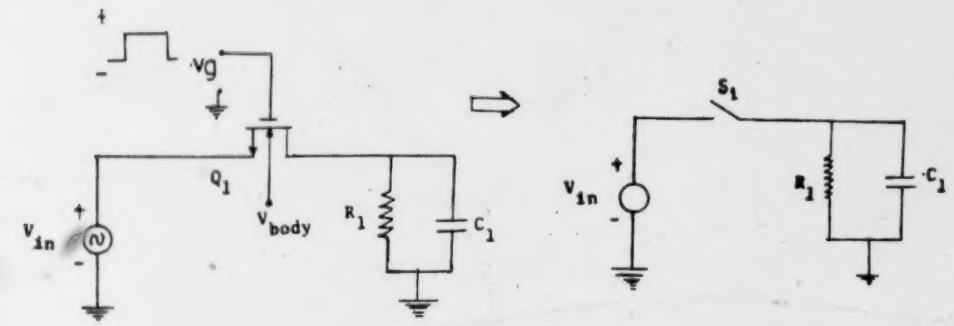


Fig.2.2 MOS transistor as ideal analog switch

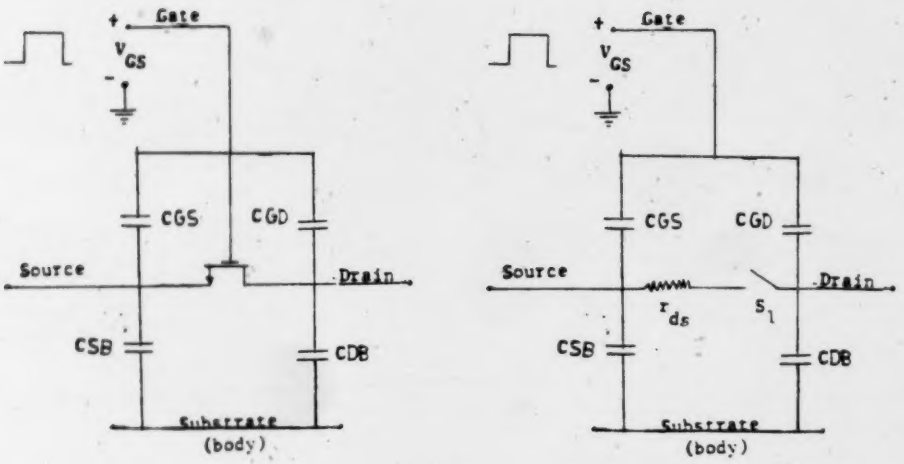


Fig.2.3 MOS transistor as nonideal analog switch

(width/length of the transistor).

The relative effects of CSB and CDB can be reduced by increasing the substrate bias. The gate-source and gate-drain capacitances are usually the most troublesome since they allow a finite amount of charge to be transferred from the control path into the signal path. This is particularly bothersome when an analog switch is used to equalize or redistribute the charge across two capacitors connected at both ends of the switch. Although the value CGS and CGD are of the order of 0.1-0.2 pF for small-area devices, the amount of feedthrough charge for large clock signals can be sufficient to cause several millivolts of voltage level charge across the capacitors connected to the switch. The feedthrough effect can be virtually eliminated, or cancelled, by using a charge-cancelling scheme, as illustrated in Fig.2.4, when an additional "dummy" switch is added into the circuit, which is driven by the complement of the clock signal.

2.2.2 Double-Throw Analog Switches

The switching of a capacitor between two voltage sources is done by using two switches which are opened and closed sequentially, in a break-before-make manner as shown in Fig.2.5. This break-before-make condition is essential to ensure that the two voltage levels, between which the capacitor is switched, are electrically isolated from each other during the switching interval. Thus, the complementary

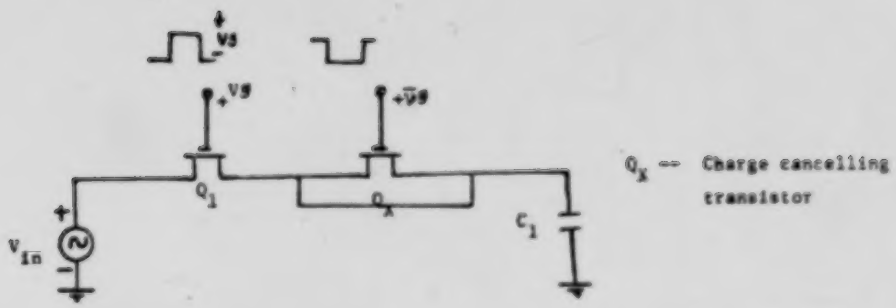


Fig.2.4 Minimum clock feed through in analog switch by use of charge canceling device

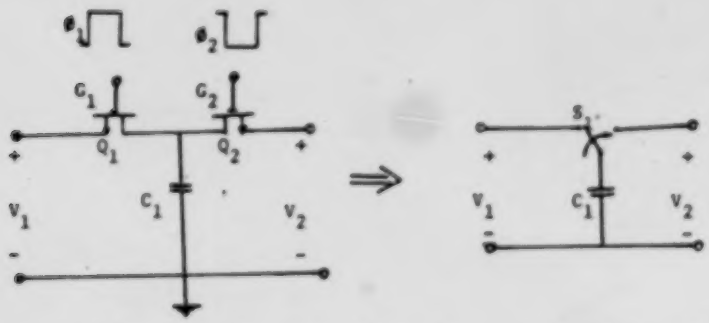


Fig.2.5 Use of two analog switches driven by non-overlapping complementary clock signals to form single pole double-throw switch

clock signals ϕ_1 and ϕ_2 applied to both switches must not have overlapping edges.

2.3 Characteristics of MOS Circuit Elements

The three essential types of circuit elements in a monolithic switched-capacitor circuit are MOS capacitors, analog switches, and operational amplifiers. In this section, the basic performance capabilities, inherent parasitics and design tolerances associated with each of these circuit elements will be reviewed.

2.3.1 MOS Capacitors

The important features of the MOS capacitor, which make it nearly ideal for switched-capacitor circuit applications, are its linearity, temperature stability, and ratio accuracy[21] . There are two basic types of capacitor structures available in MOS circuits, depending on the particular fabrication process used. These are (1) the conventional MOS capacitor structure, and (2) the double polysilicon capacitor.

The basic MOS capacitor structure is directly compatible with the conventional metal-gate CMOS processes, and requires no additional masking or diffusion steps. However, in the case of silicon-gate MOS technology, which uses deposited polycrystalline silicon (or the so-called poly layer) to form the gate electrodes of the MOS devices, the conventional MOS capacitor is not directly compatible

with the basic process, and would require additional process steps. An alternate approach is double-polysilicon capacitor which uses a thin dielectric oxide layer between two polysilicon layers, on the chip surface, to form a capacitor.

Conventional MOS capacitor structures offer better absolute-value control[21], whereas the double-poly capacitors have somewhat lower stray parasitics associated with them.

2.3.2 MOS Analog Switches

The MOS transistor makes a nearly ideal analog switch. In switched-capacitor circuit design, the MOS analog switches carry very little current. Therefore, they are normally designed as minimum-geometry devices, with minimum channel width, and a channel width-to-length ratio of unity. However, since the majority of capacitors used in switched-capacitor circuits are in the range of 1-10 pF, the parasitic capacitance associated with the analog switches must also be taken into account in calculating capacitor ratios.

2.3.3 Noise Characteristics

There are two primary sources of noise in switched-capacitor circuits. The first is due to the thermal noise of the MOS switches, and the second is due to the operational amplifiers. The qualitative effects of each of

these noise sources are briefly examined below.

2.3.3.1 Noise due to MOS switches

When a MOS transistor switch is in the on condition, connecting a capacitor C to a voltage source, the thermal noise power in the resistive channel is given by the thermal noise equation [20]

$$(V_n)^2\text{rms} = 4kTR_{on}(\Delta f)_n \qquad (2.3\text{-}1)$$

where k is the Boltzmann's constant, R_{on} is the on resistance of the channel, and $(\Delta f)_n$ is the noise-power bandwidth of the RC circuit formed by the sampling capacitor and the switch resistance R_{on}. The noise-power bandwidth $(\Delta f)_n$ associated with a single-pole low-pass circuit of resistance R_{on} and capacitor C is given as

$$(\Delta f)_n = 1/(4R_{on}C)\ \text{Hz} \qquad (2.3\text{-}2)$$

Substituting eq.(2.3-2) into eq.(2.3-1), one gets

$$(V_n)^2\text{rms} = kT/C \qquad (2.3\text{-}3)$$

When the switch is turned off, this noise is then sampled and held on the sampling capacitor.

The two important conclusions to be drawn from this qualitative discussion are as follows. To reduce noise problems associated with analog switches, one should (1) keep the sampling capacitor sizes as large as possible, and (2) minimize the number of switches in the circuit. Unfortunately, the sampling capacitor is often chosen as the smallest practical "unit capacitor", against which the other capacitors in a switched-capacitor circuit are scaled. Therefore, increasing its size is often not

practical since it leads to increased chip area.

2.3.4 Noise introduced due to sampling

The noise at the output of most switched capacitor circuits may be separated into two classes of noise voltages; 1st: sampled and held noise voltages and 2nd: direct noise which is caused by a straight path from the considered noise source to the output [16]. The sampled-and-held noise is highly undersampled, resulting in its dominance over the direct noise within the SC circuit signal bandwidth. The sample-and-held noise is due to noise samples stored in certain capacitors of a SC network. By the nature of the SC network the noise stored on the capacitors changes only at the sampling time. Input and output noise samples at the even and odd clock phases are all distinct. The total noise output is the sum of the noise sources of the individual phases. Each noise output spectrum is determined by multiplying the discrete input noise spectrum and the corresponding magnitude-squared z-domain transfer function evaluated on the unit circle[39].

The "on" resistance of the MOS switches and the operational amplifier noise are considered as the primary noise sources of switched capacitor circuits.

By the aliasing of high frequency noise components the output noise of the second and the following sampled-data stages increases.

If switched capacitor circuits with low noise are needed, it is important to choose low noise operational amplifiers and to reduce the equivalent SC resistance values as far as possible. The equivalent SC resistances can be brought down by increasing the sampling frequency or/and the values of the switched capacitors.

2.4 Practical Design Constraints

In the actual circuit implementation and interconnection of monolithic switched-capacitor circuits, a number of practical design constraints [23], [29] must be kept in mind to assure stable and reliable circuit operation. Some of these fundamental points are listed below

a. An equivalent resistor generated by switched-capacitor techniques can not be used to close an operational amplifier feedback path by itself. An operational amplifier requires a continuous-time feedback path to assure stability. Since a switched-capacitor resistor does not provide a continuous-time feedback path, it cannot be used as the only feedback path around an operational amplifier. However, it can be used in conjunction with a capacitor to shape the frequency response of the feedback path.

b. No circuit node must be left floating. All circuit nodes must have a resistive path to ground in order to avoid charge accumulation at capacitor plates. A

path formed by a switched capacitor resistor is acceptable for this purpose.

c. The bottom plates of MOS capacitors must be connected to ground or to a voltage source. The bottom-plate parasitic capacitance is in the range of 5-20% of the nominal capacitor value, and is often nonlinear in its response. It must be connected to an ac ground or be switched between voltage sources so that the charge flow in and out of the parasitic will not affect the circuit response. This rules out floating switched-capacitor configurations, capacitive voltage dividers comprised of three or more capacitors, or circuits which sequentially switch both ends of a capacitor into an operational amplifier input.

d. The noninverting operational amplifier input should be kept at a constant voltage. If the positive input of the operational amplifier is connected into the signal path, then the inverting input no longer behaves as a virtual ground, and the filter response becomes sensitive to all parasitic capacitance due to substrate capacitance, bus lines, and switches connected to the inverting input.

2.5 Applications and Limitations of Switched-Capacitor Circuits

Switched-capacitor circuit design techniques, together with the advances in analog design, have made it possible to implement a wide range of functions on the silicon chip. The biggest advantage of switched-capacitor circuits, compared to conventional active-RC circuits, is the elimination of the need for precise control of capacitor and resistor absolute values. Instead, the performance is determined by capacitor ratios and the choice of the clock or sampling frequency fc. Normally, the clock signal is either supplied externally or derived from an on-chip oscillator and countdown circuitry.

There are two practical limitations to monolithic switched capacitor circuits: high-frequency capability and noise characteristics. The high-frequency capability is limited by the clock frequencies that can be used in practical circuits. The practical choices for fc are limited to no more than several hundred kiloHertz .

2.6 Application of Switched-Capacitor Resistor in RC oscillators

The magnitude of a switched-capacitor resistor is controlled by varying the switching frequency. Their use in RC oscillators enables the variation of the frequency of oscillation by changing the relatively high switching frequency. Since the high switching frequency is easily

voltage-controlled[61], the low-frequency oscillator effectively becomes a V.C.O giving a low-distortion sinusoidal waveform.

The magnitude of the resistance Req, obtained by switching a capacitor Cr at a frequency fc, is given by

$$Req = 1/(fc\ Cr) \qquad (2.5\text{-}1)$$

The frequency of a Wien-bridge oscillator (Fig.2.6), using a pair of ganged resistors(R) and capacitors (C), is given by

$$f = 1/(2\pi\ C\ R) \qquad (2.5\text{-}2)$$

If the resistors R are replaced by switched capacitors Cr, for Cr< C, we can combine eqs.(2.5-1) and (2.5-2), giving

$$f = (1/2\pi)(Cr/C)fc$$

or

$$f/fc = (1/2\pi)(Cr/C) \qquad (2.5\text{-}3)$$

Thus the frequency of the oscillator is linearly related to the switching frequency fc and the constant of proportionality is accurately defined by the ratio of the capacitors (Cr/C). For example, let C=10nF and R=10k(ohms), which gives f=(10/2 π)kHz. Assuming a switching frequency of 1 MHz, the value of Cr required to obtain a resistor of 10k(ohms) is 100pF. Thus (fc/f) = 200 π.

2.6.1 Design considerations

2.6.1.1 Switching arrangement

The resistors R that are to be varied simultaneously can be replaced by switched capacitors Cr. The switching arrangement employs four analogue

switches depicted as two single-pole-double-throw switches in Fig.2.7. The switches are operated using a two-phase (nonoverlapping) clock of frequency fc.

2.6.1.2 Switches

The upper limit to the oscillation frequency is set by the maximum frequency at which the switches can be operated. The on-resistance R_{on} of the switch places an upper limit on Cr, since Cr_{mx} R_{on} << tp for the capacitor to charge and discharge completely.

2.6.1.3 Choice of capacitors

Let the sum of feed-through capacitance of the switch, parasitic junction capacitance and the strays present in the circuit be Cjs. Thus Cjs << Cr << (tp/R_{on}). The maximum value of the capacitor C (C_{mx}) that can be used is limited by its own self time constant τ_s , since (τ_s/C) should be greater than R_{mx},the maximum resistance which can be simulated. Thus the R_{mx} achievable is controlled by the off resistance Roff of the switches or (V_{mx}/Ib) of the O.A. The ratio (C/Cr) should be large (>100) for the approximation to be valid and to give a smooth sinusoidal waveform. The value of the (C/Cr) ratio that can be employed in practice is of the order of 10^2, and thus the ratio (fc/f) attainable is $2 \pi 10^2$. The ratio $Roff/R_{on}$ of FET switches is of the order of 10^7.

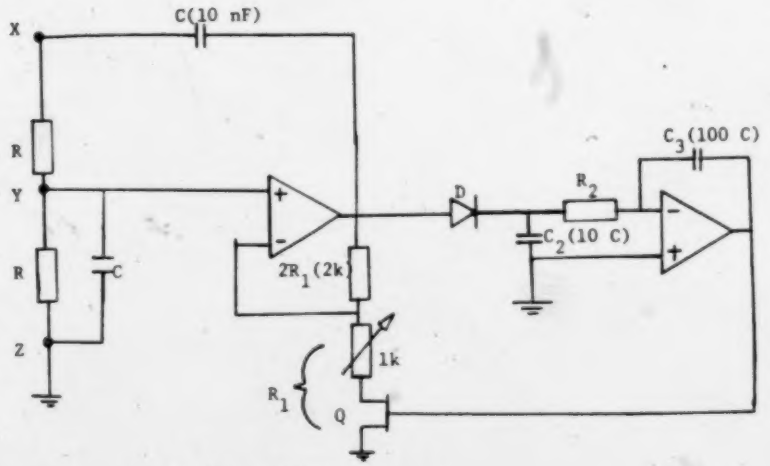


Fig.2.6 Wien-bridge oscillator

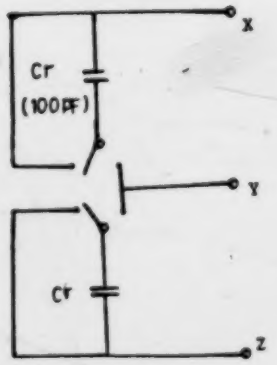


Fig.2.7 Switching arrangement

2.7 MOS operational amplifier

There have been numerous barriers to the development of useful all-MOS operational amplifiers. Compared to bipolar transistor technology, MOS yields matched pairs of transistors with an order of magnitude higher offset voltage and an order of magnitude lower transconductance per stage. MOS transistor equivalent input noise is much higher, particularly the 1/f component. Despite recent improvements in every area, MOS operational amplifiers can not compete with the performance characteristics of their bipolar transistor counterparts; stand-alone MOS operational amplifiers are unlikely to challenge the position of general-purpose bipolar transistor op amps as small-scale integrated circuits. Nevertheless, the MOS amplifiers are very attractive as components on large-scale integrated MOS circuits. This is true because MOS op amps are three to five times smaller in area than their bipolar counterparts, and, more importantly, because they are technologically compatible with the other circuit elements.

Improvements in MOS process control have reduced the typical input-offset voltage of MOS matched pairs to the order of 5-10 mV. This is still too high for many critical analog applications. However, sampled-data techniques can provide one to four orders of magnitude reduction in effective offset[19].

2.7.1 Example of a CMOS operational amplifier

The schematic diagram of a relatively simple CMOS op amp is shown in Fig.2.8. Transistors M5, M6, M9, M10, and M11 provide current-source biasing of the remaining circuitry. M1 through M4 form an amplifier with differential input and single-ended output; common-mode signals are rejected. M8 forms the second and last amplifying stage. M7 and C provide internal phase compensation without undesirable output loading or signal feedforward. Die area for this amplifier is 0.35 mm² in a standard metal-gate CMOS process [24]. Performance parameters are as listed below.

CMOS op amp performance:

Unity-gain BW: 3.2 MHz

Slew rate : ± 8/33 V/μs

Circuit Area : 0.35 mm²

Openloop gain: 1500

Input offset : < 20 mV

RMS input noise: 51 μV

Power consumption : 22 mW

For applications in SC oscillators, the op amp must have enough gain-bandwidth product to meet the gain requirements (with negligible phase shift) at the highest oscillation frequency. The input-offset voltage has no appreciable effect. The amplifier settling times must be adequate to accomodate high sampling rates. Further discussion of the op amp usefulness in oscillator circuits appears in the following chapters.

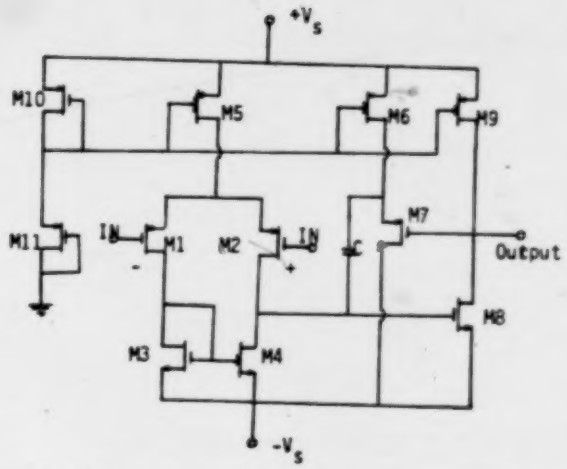


Fig.2.8. Schematic diagram of a simple CMOS operational amplifier.

3. SWITCHED CAPACITOR INTEGRATORS

For applications in amplitude control systems, instantaneous integration of a pulse is required. This can be done using a switched capacitor integrator. Fig.3.1 shows the switched-capacitor equivalent of a conventional lossless RC integrator circuit. By substituting SC equivalence for resistor R_1, the transfer function of the switched-capacitor integrator can be written as

$$\frac{Vout}{V_1}(jw) = \frac{-fc.C_0/C_1}{jw} \qquad (3.1\text{-}1)$$

for frequencies where $w << wc\ (=2\pi fc)$.

3.1 Effects of Parasitic Capacitances

In addition to bottom-plate parasitics, the other circuit parasitics are the stray capacitance associated with the top plate, metal interconnection paths, and the analog switches. The effect of these circuit parasitics can be examined using the simple switched-capacitor integrator circuit of Fig.3.1, where all the basic parasitics associated with the circuit nodes are shown separately.

Cp_1 is the parasitic source-substrate capacitance of the analog switch transistor Q_1, Cp_2 and Cp_3 are the drain-substrate capacitances of Q_1 and Q_2 as well as the top-plate and interconnection parasitics associated with C_0. Cp_4 is the source-substrate capacitance of Q_2 and the input capacitance of the operational amplifier. Cp_5 and Cp_6 are the top- and bottom-plate parasitics associated with the

integrator capacitance C_1. The bottom-plate parasitic Cp_4 has no effect on circuit performance since it is driven from the operational amplifier output. Cp_1 is in parallel with the voltage-source input. Cp_4 and Cp_5 are in parallel with the virtual ground node (inverting input) of the operational amplifiers. Therefore, they do not affect circuit performance as long as the input signal source impedance is very low and the operational amplifier gain is high. The parasitic capacitances Cp_2 and Cp_3 are in parallel with the switched capacitor C_0; therefore, they directly affect the circuit performance by causing C_0 to have an apparent value of C_0', where

$$C_0' = C_0+Cp = C_0(1+r_0) \qquad (3.1\text{-}2)$$

where $Cp = Cp_2 + Cp_3$ is the total parasitic capacitance associated with the top plate of C_0, and $r_0 = Cp/C_0$ is the fractional parasitic top-plate capacitance associated with C_0

The effect of the parasitic top-plate capacitor is to modify the integrator gain constant by a factor of $(1 + r_0)$, such that the basic transfer function for the circuit of Fig.3.2b becomes[21]

$$[Vout/V_1] = -(fc\ C_0'/C_1)/jw = [(fcC_0/C_1)(1+r_0)]/jw \qquad (3.1\text{-}3)$$

The detrimental effects of top-plate parasitics can be greatly reduced by using dual-switch equivalents of the simple switched-capacitor stage, as shown in Fig.3.3.

It can be shown that the equivalent average current carried across the switched capacitor is equal to

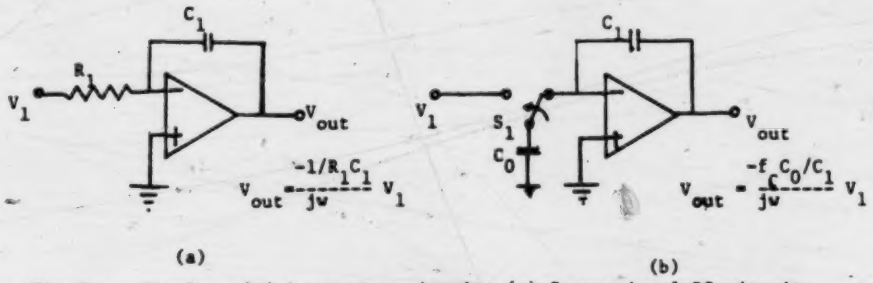
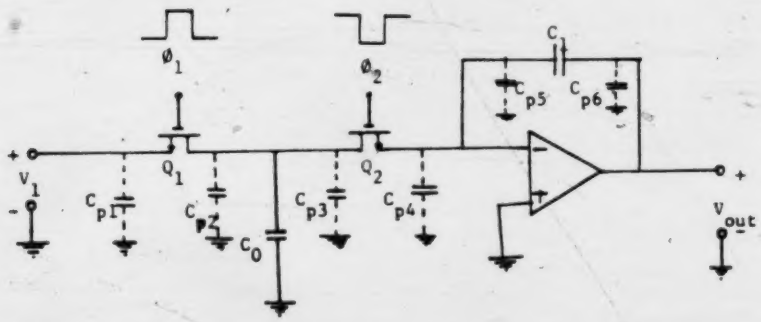
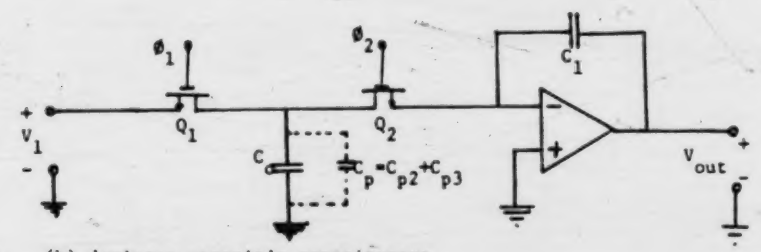


Fig. 3.1 Single-ended integrator circuit. (a) Conventional RC circuit
(b) its switched capacitor equivalent



(a) Locations of parasitic capacitances



(b) dominant parasitic capacitances

Fig. 3.2 Effects of parasitic capacitances in switched capacitor integrator

$$I_{eq} = Q_o f_c = f_c C_o (V_1 - V_2) \qquad (3.1\text{-}4)$$

for the circuit of Fig.3.3a. In the case of the circuit of Fig.3.3b, the equivalent average current is

$$I_{eq} = -f_c C_o (V_1 + V_2) \qquad (3.1\text{-}5)$$

which is equivalent to inverting the polarity of the input voltage V_1.

3.2 Frequency Limitations of SCC's

Designing SC circuits for applications in frequency bands beyond 100 kHz becomes problematic because the amplifiers and switches can no longer be considered ideal. The amplifier's finite gain and finite bandwidth influence the SC circuits behaviour [14].

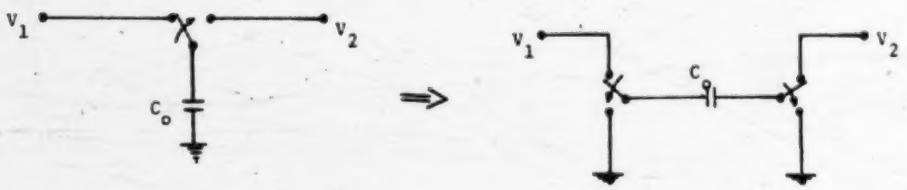
3.2.1 Influence of Amplifier Finite Gain and Bandwidth and switch-on Resistances:

Given an integrators amplitude and phase errors, the deviation of the frequency response of a given circuit structure can be calculated. Among the networks realizing a time-discrete integrator, we select two that are principally different, namely the strayinsensitive integrator and an integrator consisting of a unity-gain amplifier.

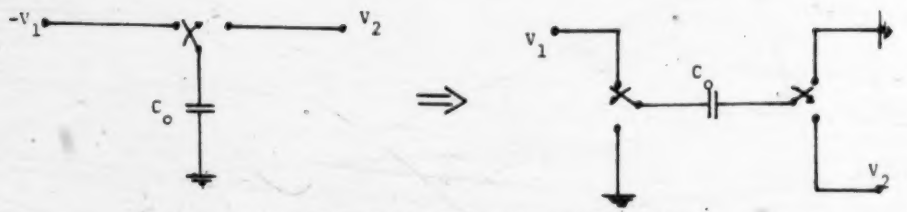
3.2.1.1 Stray-Insensitive Integrators:

Fig.3.4 shows the well-known circuit realizing a stray-insensitive noninverting integrator.

In the analysis of the integrator network the amplifier and the switches of the circuit are replaced



(a) Noninverting configuration



(b) Polarity inverting configuration

Fig.3.3 Dual-switch equivalent of simple switched-capacitor stage

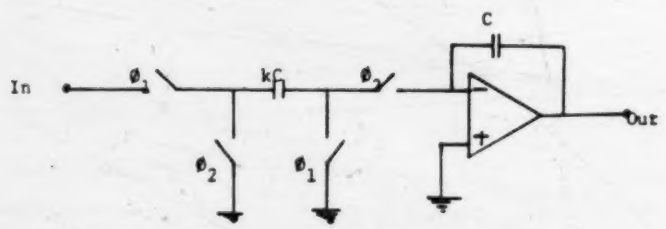


Fig.3.4 Noninverting stray-insensitive SC integrator

during each phase by the linear models shown in Fig.3.5. The values of all necessary voltages are then evaluated at the end of each phase, resulting in a set of difference equations, which can readily be Z-transformed [17]. Finally, the error function E(z) is extracted from the Z-domain transfer function according to the following equation:

$$H(z) = H(ideal)(z)\ E(z)$$

$$E(z)\Big|_{z=\exp(jw.tp)} = [1+m(w)]\exp[j\theta(w)] \qquad (3.2\text{-}1)$$

tp : clock period

$m(w)<<1$: magnitude error

$\theta(w)<<1$: phase error.

The detailed calculation of the integrator error function E(z) is rather tedious and is therefore relegated to the Appendix II. Here, we shall show the final results. In the following equations ϵA is defined as the inverse of the amplifier gain (i.e., $1/A_0$) and ϵ_k is the exponent of the ratio -tc/tk.

Depending on the switching phase of the integrator output signal, two slightly different solutions for the error function E(z), or m and θ, respectively, are obtained. Letting Eij be the error incurred when the input phase is i and the output phase j, we have (see Appendix II)

$$m_{1,1}(w) = (1/1+k)[(k/2)(1-\alpha)-k(1-\beta) -\epsilon A(1+\beta k)-2\epsilon_k]$$

$$\theta_{1,1}(w) = \text{arc tan}\{(k/1+k)[(1-\alpha) / (2\tan (wtc))]\}$$

$$m_{1,2}(w) = (1/1+k)\{(k/2)(1-\alpha)-(1-\beta)\ (1+k)$$

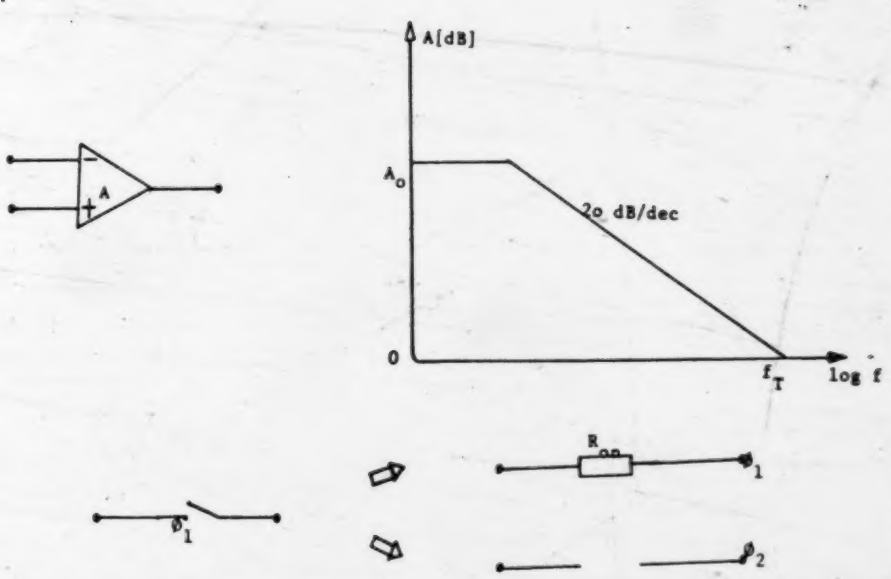


Fig. 3.5 Models for amplifier frequency response and switch resistance

$$+\beta[(\alpha/\beta)(1-2\epsilon_k)]\cos(w.tp)\}$$

$$\theta_{12}(w) = \arctan\{(k/1+k)\,[(1-\alpha)/(2\tan(wtc))]\}-(1/1+k)\{(\alpha/\beta)(1-2\epsilon_k)-1\}\sin(w.tp) \qquad (3.2\text{-}2)$$

In the numerical example, the signal frequency w has been assumed to equal $w_o = wc/12.5$, a value that lies within the typical operating range of an SC network. Besides, the magnitude errors are practically frequency independent within the frequency range in which w tp << 2 π holds.

We can notice a correlation between the influence of the switch-on resistances Ron and the amplifier bandwidth fT , which increases for decreasing values of the two variables fT/fc and tc/tk, where,

fT/fc : ratio of amplifier bandwidth fT to clock frequency

tc/tk = 1/(2 fc kC 2 Ron): ratio of active clock phase (tc = tp/2) to RC time constant tk.

This correlation is due to the fact that the switch-on resistances also influence the time behavior of the differential input voltage of the amplifier, which in turn directly determines the output voltage of the integrator. In order to keep the values of the three critical error functions m_{11}, m_{12}, and θ_{12} smaller than 1 percent, the following three inequalities must be fulfilled:

$$A_o \geq 1000$$

$$f_T/f_c \geq 2 \qquad (3.2\text{-}3)$$

$$t_c/t_k \geq 10$$

With today's technology, $f_T/f_c \geq 2$ implies the most stringent limitation for stray-insensitive SC networks. For a 2 MHz amplifier, for instance, the maximum tolerable clock frequency would be 1 MHz, whereas the third inequality would allow a maximum clock of 2.5 MHz (assuming kC= 1 pF and Ron = 10 k ohms). Since the gain of a typical MOS amplifier exceeds 60 dB, the first inequality implies practically no restriction at all.

3.2.1.2 SC Integrators with Unity-Gain Amplifiers

Unity-gain amplifier circuits are less affected by the finite gain-bandwidth product than their conventional inverting op amp counterparts. However, this advantage must be paid for with a high sensitivity to parasitic capacitances. Also, the switch-on resistances cause more problems here because the capacitor values must be relatively large in order to keep the influence of the parasitic capacitances as small as possible.

Considering the two unity-gain integrator circuits in Fig.3.6, we note that both have two stray-sensitive nodes. The corresponding parasitic capacitances are indicated as $\epsilon_k C$ and $\epsilon_s C$, respectively. Taking into account the switch-on resistances as the only error source, the transfer function of both circuits is affected by the following error function:

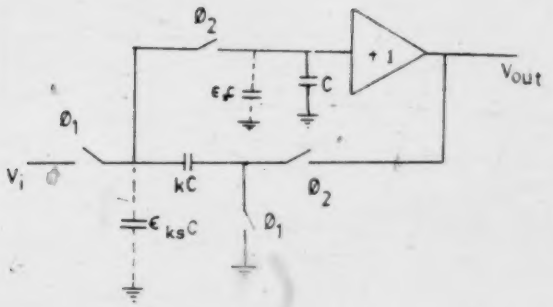


Fig. 3.6a Noninverting integrator

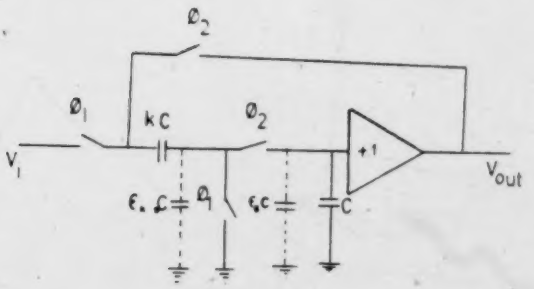


Fig.3.6b Inverting integrator

$$E(z) = 1-2\epsilon_k \qquad \text{with} \qquad \epsilon_k = \exp(-tc/tk) \qquad (3.2\text{-}4)$$

$$tk = 2Ron\ kC.$$

Thus, in this simplified case, the integrator performance is deteriorated only by a magnitude error $mr=-2\epsilon_k$. In order to compare this result with the influence of the parasitic capacitances, we again express the corresponding deviations in terms of our error function E(z). Assuming ideal switches and amplifiers and applying the principle of charge conservation to the two stray-sensitive circuits, we obtain the following error functions:

3.2.1.3 Inverting integrator

$$E_{12}^{-}(z) = (1-\epsilon_s)[\ (1-z^{-1})/(1+\epsilon_{ks}-z^{-1})\ ]$$

$$m_{12}^{-}(w) = -(\epsilon_s+\epsilon_{ks}/2\ ) \qquad (3.2\text{-}5)$$

$$\theta_{12}^{-}(w) = \epsilon_{ks}/(2\tan(wtc))$$

3.3 Discrete-Time Effects

Using sampled-data techniques, the exact transfer function of a Switched Capacitor Integrator, such as the one shown in Figure.3.1b, can be expressed as

$$\frac{Vout}{V_1}(jw) = -\left[\frac{fcC_0/C_1}{jw}\right]\left[\frac{w.tp}{2Sin(w.tp/2)}\right]\exp-(jw.tp/2) \qquad (3.3\text{-}1)$$

Where tp (= 1/fc) is the period of the clock signal

Comparing eq.(3.3-1) with the simplified result given in eq(3.1-1) one sees that the exact expression differs from the approximate response by both an amplitude and a phase error. In the limit, as the switch frequency increases such

that w tp approaches zero, both of these error terms approach unity and the response reduces to the case of the ideal RC integrator.

The amplitude error is usually of very little concern in the frequency of interest where w tp << 1. The phase error, which represents a phase delay proportional to frequency, is the most bothersome. This phase shift or delay is due to the one-half clock cycle delay in replenishing the charge on the capacitor C_o in Figure 3.1b. Typically, the effect of this excess phase is in the form of Q-enhancement, or undesired peaking, in the circuit response. The phase error or the delay term associated with eq.(3.3-1) can be compensated by one of two approaches:

1. By using predistortion technique. The circuit can be "predistorted" in actual design so that the response is the desired one when the excess phase is present. This approach requires fairly extensive numerical calculations[45], and has the disadvantage of increasing the component sensitivity and the design complexity in circuits requiring transmission zeros in the response.
2. By adjusting the phasing of clock cycles between successive integrator stages, using the so-called lossless digital integrator, or LDI, clocking scheme. In this scheme, the clock phases are arranged so that the delay time through every other integrator is reduced by one-half clock cycle.

4. OSCILLATORS

Because all SC circuits require a clock that is an oscillator, one may wonder about circuits that use something to create the same thing. However, there are several good reasons for examining SC oscillators. One of these reasons is that the clock frequency is a square wave whose frequency is generally very high. We shall see that the SC oscillator is in effect a frequency divider resulting in a lower frequency sinusoid. It will be shown that the frequency division ratio is not restricted to integer. Another reason to examine SC oscillators is to achieve quadrature oscillation, which leads to phase-shifting networks. For many oscillator applications, the frequency of the oscillator should be variable. The clock oscillator provides a convenient means of tuning the oscillation frequency of the SC oscillator. Finally, SC oscillators can provide precise waveforms from an imprecise clock.

The first category of oscillators considered is called the tuned oscillator. The RC oscillator is a subcategory of this class of oscillators. The tuned oscillator is almost a pure sinusoid and typically has very good frequency stability. It requires tuned circuits to maintain the frequency. The amplitude is determined by some form of soft-limiting, which can require a complex circuit. One of the disadvantages of the tuned oscillator is that it is difficult to vary the frequency. LC oscillators and quadrature oscillators also belong in the tuned oscillator

class. The tuned oscillator works on the principle of having the open loop gain of a feedback loop become exactly 1 with 0° phase shift at the desired frequency of oscillation.

Another subcategory of oscillators called multiphase oscillators use multiphase rectifiers. Since MOS technology does not provide multiphase rectifiers, Sequence Discriminator (SD) oscillators and two-integrator oscillators which does not require rectifiers are covered in this chapter. These multiphase oscillators can be realized using SC techniques.

The second category of oscillators is called the untuned oscillator. These oscillators can produce nonsinusoidal waveforms. However, simple circuits that can shape a sinewave from the untuned oscillator are available. For this reason, the principle of untuned oscillators is also included in this dissertation for completeness.

The parameters which are often used to describe an oscillator are briefly explained in the following paragraphs. Wien-bridge, Twin-T, multiphase, and untuned oscillators are discussed in the subsequent sections. At the end of this chapter frequency stability as applied to SC oscillators is explained.

Amplitude of Oscillations:

The exponential build-up of the oscillator will continue as long as the average gain over the cycle is greater than the threshold value. To prevent this the amplitude of the oscillator is determined by a regulating network. The

amplitude regulating networks are discussed in the next chapter.

Distortion of waveform:

The self-starting oscillator drives itself into limiting and in the process distorts the sinusoidal output signal. To avoid distorting the output signal, the degree of nonlinearity must be kept minimum.

Frequency Stability:

The frequency of oscillation is identically that frequency at which the net phase shift around the amplifier and feedback loop is zero. All oscillators are to some degree susceptible to frequency changes caused by the resistive loading of the frequency selective network. Since the feedback network contains reactive elements, the insertion of any resistance will change the phase response and also the null frequency.

Wien-bridge Oscillator:

Fig.4.1 shows the analog form of a Wien-bridge oscillator. Our approach is simply to replace the resistors with an appropriate SC simulation. One possible circuit is shown in Fig.4.2. The frequency of oscillation of the Wien bridge oscillator of Fig.4.1 is given as[1]

$$w_o = 1/RC \qquad (4.1\text{-}1)$$

and the gain necessary for oscillation is

$$k = 1+(RA/RB) \qquad (4.1\text{-}2)$$

Replacing the two resistors designated as R by parallel SC resistors results in Fig.4.2. For the moment, we shall ignore resistors RA and RB, we shall show how they can be realized shortly. Analysis of the transfer function of the SC feedback network, assuming that fc >> f_o results in

$$[Vi(s)/Vout(s)] \simeq [s.tp(C/CR)]/[(s.tp.C/CR)^2+(3s.tp.C/CR)+1]$$

$$= (sCR/tp\ C)/[s^2+(3sCR/tp\ C)+(CR/tp\ C)^2] \qquad (4.1\text{-}3)$$

Therefore the frequency of the oscillator is

$$w_o \simeq CR/(C\ tp) = (CR/C)fc \qquad (4.1\text{-}4)$$

We can now see how the clock frequency can be used to control the oscillator frequency. The result is essentially a frequency division of fc by the factor $2\ \pi$ C/CR. An important component that is missing from both oscillators is the amplitude regulating circuit. These circuits are discussed in the next chapter .

An oscillator similar to Fig.4.1 is shown in Fig.4.1a. An SC realization of this oscillator is shown in Fig.4.1b. If $C_1=C_4=CR$ and $C_2=C_3=C$, then it can be shown[1] that

$$fosc \simeq (1/2\pi)(CR/C)fc \qquad (4.1\text{-}5)$$

It is well known that the Wien-bridge oscillator circuit with the gain of the feedback amplifier adjusted to be less than three becomes a second-order bandpass active filter.

Twin-T Oscillator:

A non ideal twin-T coupled with a finite gain amplifier can produce oscillations. The required amplifier gain can be

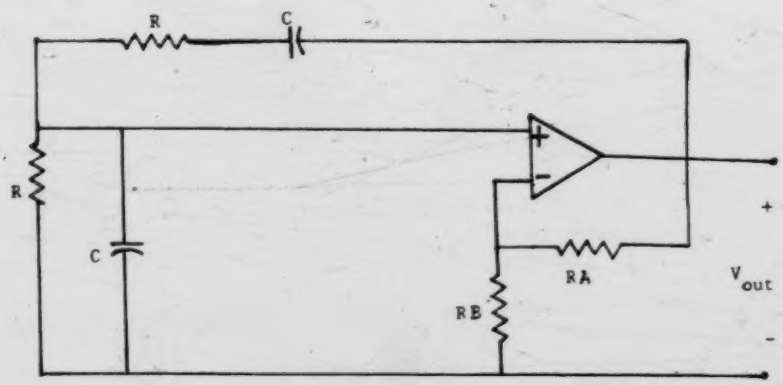


Fig. 4.1 Analog form of a Wien-bridge RC oscillator

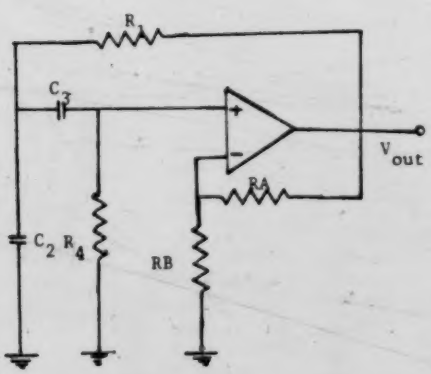


Fig. 4.1 (a) A RC oscillator

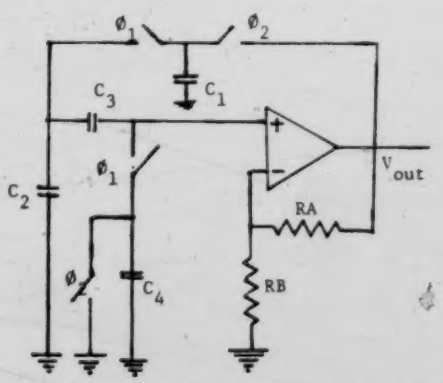


Fig. 4.1 (b) A SC realization of (a)

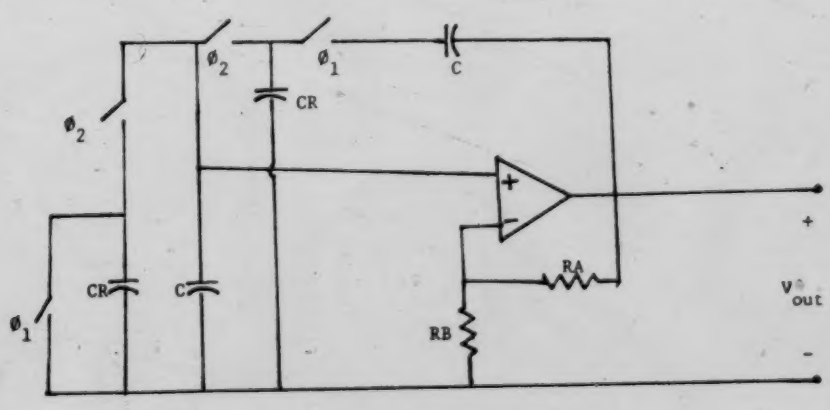


Fig. 4.2 SC realization of Fig. 4.1

positive or negative depending on the type of imperfection of the twin-T. In this section, a systematic procedure is outlined to find out the minimum amplifier gain required to sustain oscillations as well as the frequency at which the circuit will oscillate, knowing the nominal values of each component of the passive twin-T. In the following discussion the switched capacitor resistors are treated as continuous resistors (assuming clock frequencies to be far greater than signal frequency). This is because no analysis methods, known to-date, are available for a mixed continuous and switched capacitor circuits[10,48,56,64].

The most widely known twin-T (Fig. 4.3) has the following Y parameters.

$$[Y] = [1/2R(sRC+1)]\begin{vmatrix} s^2(RC)^2+4sRC+1 & -s^2(RC)^2-1 \\ -s^2(RC)^2-1 & s^2(RC)^2+4sRC+1 \end{vmatrix} \quad (4.1\text{-}6)$$

The resulting open-circuit voltage-transfer function follows as:

$$T(s) = -y_{21}/y_{22} = [s^2(RC)^2+1] \,/\, [s^2(RC)^2+s(4RC)+1] \quad (4.1\text{-}7)$$

This is a second order transfer function with two negative real poles P_1, P_2 and two conjugate imaginary zeros Z_1, Z_2. This is illustrated in Fig.4.4 along with the well known amplitude response of this ideal circuit.

A disagreement on the ideal twin-T phase response seems to exist in the literature since at w_n, the null frequency , the phase is shown as being either 0° or -180°. In fact both interpretations may be right, the assumption of an ideal

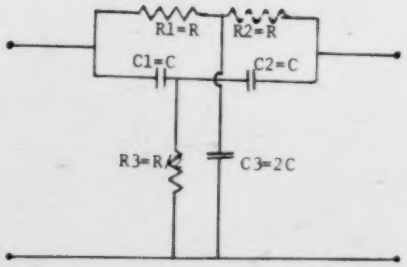


Fig. 4.3 The ideal symmetrical twin-T.

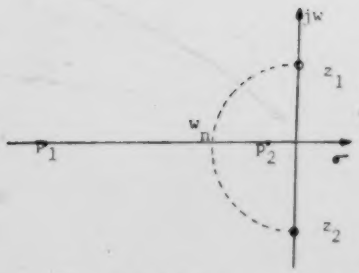
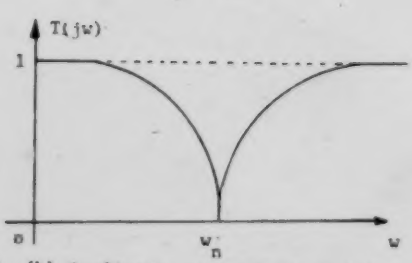


Fig. 4.4 (a) Pole-zero diagram



$s = \sigma + jw$

$w_n = 1/RC$

$z_i = +/- jw_n$

$p_i = (-2 +/- \sqrt{3})w_n$

Fig.4.4 (b) Amplitude response of an ideal symmetrical twin-T.

network results in a phase ambiguity at w_n. This can be seen in (4.1-8) which is the voltage-transfer function (4.1-7) where s=jw.

$$T(jw) = \{1-(wRC)^2\}/\{[1-(wRC)^2]+j4wRC\} \qquad (4.1\text{-}8)$$

The phase of the denominator varies between 0° and 180°, being 90° at $w=w_n$. The phase of the numerator, on the other hand, is 0° for $w<w_n$ and either 180° or -180° for $w>w_n$. There are, therefore, two admissible phase responses for an ideal symmetrical twin-T; these are shown in Fig.4.5, where it can be seen that the mean phase value at $w=w_n$ could be either 0° or -180°.

4.1 The NonIdeal Symmetrical Twin-T

Because of the existing deviations between the actual and the ideal values of the components in a practical twin-T circuit, the positions of the poles and zeros of its transfer function will fluctuate around their nominal positions shown in Fig.4.4a. Most important are the zero positions' fluctuations. The zeros of the ideal twin-T lie exactly on the imaginary axis while those of the non ideal circuit may fall in the left half-plane (LHP) or in the right half-plane (RHP). In both cases (Fig.4.6), the amplitude response no longer shows an infinite null at a frequency w_n but instead a finite attenuation value x at a frequency w_n', the new maximum rejection frequency. The values of x and Δw_n ($\Delta w_n=w_n'-w_n$) is related to the deviations of the components values from their ideal ones.

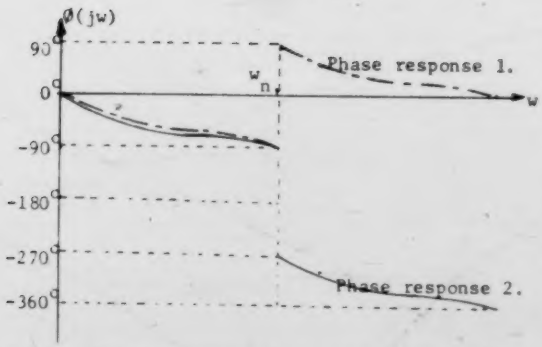


Fig.4.5 Phase response of an ideal symmetrical twin-T.

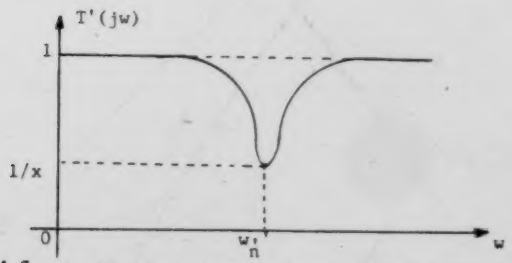


Fig.4.6 Amplitude response of a nonideal symmetrical twin-T.

The larger the difference between the actual and the ideal positions of the zero, the larger the terms $1/x$ and Δw_n will be.

When the zeros lie in the LHP, the phase response stays within the -90° to +90° range, being 0° at w_n'; in the RHP case, the phase goes from 0° to -360°, being -180° at w_n'. This is illustrated in Fig.4.7.

The two following situations must then be considered during the design phase of an oscillator using a twin-T as the feedback network of an amplifier.

LHP Case:

With the twin-T zeros lying in the LHP, the amplifier must have a minimum gain of x and a 0° phase shift.

But this configuration is unserviceable and should be discarded. From circuit theory it is known that only circuits with non-minimal phase shift should be used for oscillators.

RHP Case:

In this case the amplifier must again have a minimum gain of x but this time a -180° phase shift.

It can be shown[7] that the more the R3 nominal value is increased, the lower the amplifier required gain for oscillations is. However the frequency stability requirement of the oscillator forces the zeros to be as close as possible to the imaginary axis for a well-defined phase step in the vicinity of w_n' (compare Fig.4.5 with Fig.4.7).

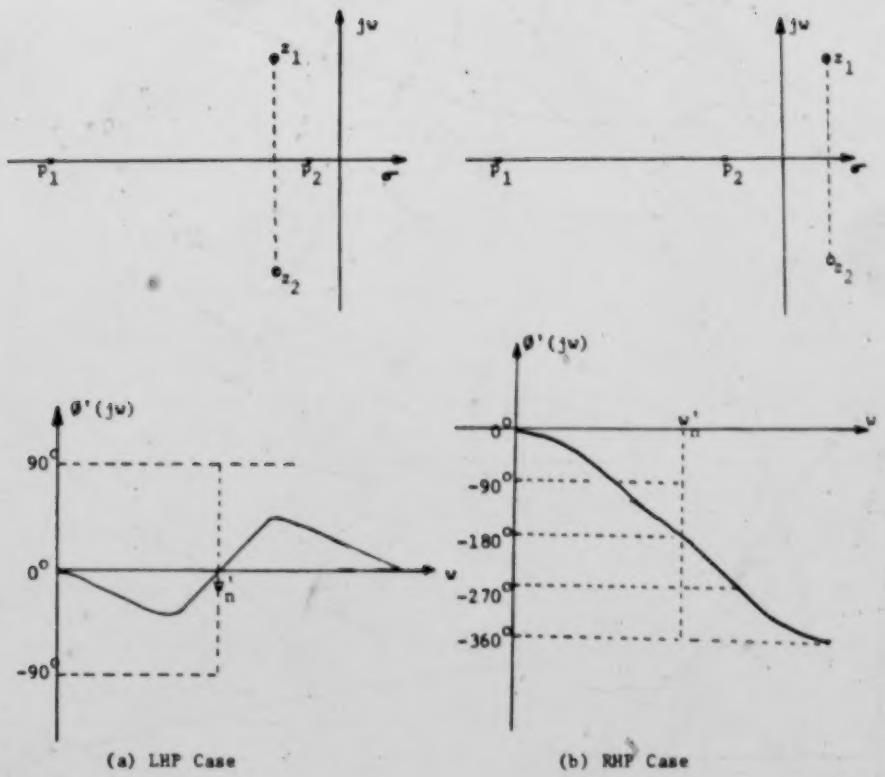


Fig.4.7 Pole-zero diagrams and phase response of a nonideal symmetrical twin-T.

There is an apparent conflict here, that is a large increase in R3 nominal value would insure oscillations with a low gain amplifier while a small increase would contribute to maintain a good frequency stability. In the latter case, however, an amplifier with both high gain and 0° phase shift at w_n would be required. This can be solved by the amplitude control circuit compulsory to obtain a good quality sinusoidal output. Such circuit normally act on the amplifier gain, here it should control the R3 value, optimizing it dynamically in order to keep the twin-T zeros as close as possible to the imaginary axis while sustaining oscillations.

Let us now consider two configurations of the twin-T oscillator. One way of realizing the gain K amplifier is to use an op-amp. Again two cases must be distinguished.

a) RHP Case

Here, the op-amp must be used in an inverting configuration since -180° phase-shift is required. Fig.4.8a shows a possible realization among others. The SC equivalent of Fig.4.8a is shown in Fig.4.8b.

b) LHP Case

Assuming that the twin-T (Fig.4.8c) is ideal and that it has the open-circuit voltage-transfer function given by (4.1-7), the following transfer function results[46].

$$v_i/v_o=\{[s^2(RC)^2+1] / [s^2(RC)^2+s(4RC)+1]\}-\alpha \qquad (4.1\text{-}9)$$

where

$$\alpha = R1/(R1+R2) ; \qquad 0\leq\alpha\leq1 \qquad (4.1\text{-}10)$$

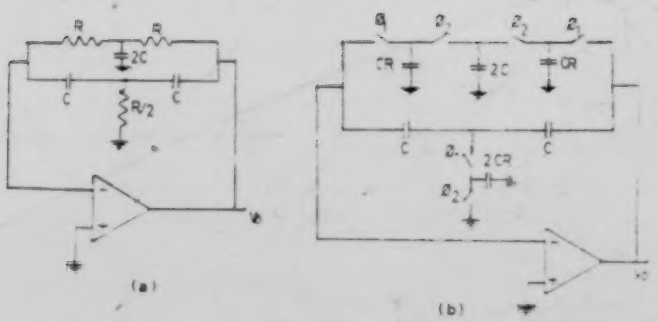


Fig. 4.8 Twin-T Oscillator (a) RC circuit (b) SC circuit. (RHP Case).

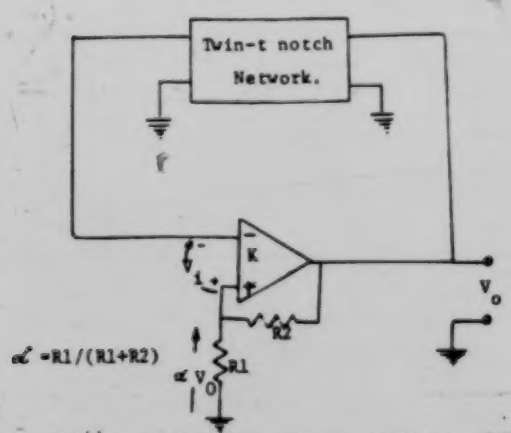


Fig.4.8(c) Dual feedback twin-T oscillator (LHP Case).

or

$$v_1/v_o=[s^2(RC)^2(1-\alpha) -s(4\alpha RC)+(1-\alpha)]/[s^2(RC)^2+s(4RC)+1] \qquad (4.1\text{-}11)$$

This transfer function has the same poles as the ideal twin-T considered by itself. The position of the zeros however is different. They are located at:

$$Z_{1,2}=[2\alpha/RC(1-\alpha)]\pm \{[\sqrt{4\alpha^2-(1-\alpha^2)}]/RC(1- \alpha)\} \qquad (4.1\text{-}12)$$

With $\alpha=0$, the circuit becomes the original ideal twin-T and the zeros are located at $\pm j/RC$ as expected. For $1/3 \leq \alpha \leq 1$, the zeros are real, and the circuit presents no interest.

For values of α between 0 and 1/3, the zeros are complex and they lie in the RHP. They go deeper in the RHP as α is increased toward 1/3.

Now, if the twin-T we are using is not ideal but has its zeros in the LHP, the addition of resistors R1 and R2, would, if α is correctly adjusted, push back the zeros in the RHP, allowing an inverting amplifier to be used.

The zero's position can be controlled in varying a twin-T component, like R3, around its nominal value. In conclusion, in the case of dual feedback, one path is formed by a resistive voltage divider, the other by a RC/SC network. The zeros of the RC/SC network can be located in the LHP, RHP, or on the w axis. However, locating the zeros in the RHP yields low distortions and unique frequency of oscillations.

4.2 RC Multiphase oscillators

In this section the circuits which produce multiphase oscillations are described. The Sequence Discriminator (SD) proposed by Wasfy [43] is given in Appendix.IV. The SD and two-integrator loop can be used to generate multiphase oscillations. The SD is an n-path symmetric network. A sequence has equal amplitude and equally spaced phase. A sequence can be represented by a positive sequence (TP) and a negative sequence (Tn) as explained in the Appendix.IV. The SD functions as a frequency selective network. Thus making it suitable for realization of an oscillator.

4.2.0.1 Three-phase and six-phase oscillators

From Tp and Tn, Y_1 and Y_2 may be chosen as

$$Y_1 = G + jwC \qquad (4.2\text{-}1a)$$

$$Y_2 = 2\ jwC \qquad (4.2\text{-}1b)$$

The circuit of this oscillator, including the SD and the feedback circuit, is shown in Fig.4.9a. Its characteristic equation, assuming A1 = A2 = A, is given by

$$D(s) = (sRC)^3(3A^2+9A+9)+sRC(6A+6)+(A^2+A+1) \qquad (4.2\text{-}2)$$

where A is the amplifier gain in the feedback circuit.

The required condition for sustained oscillations is satisfied when A = -1. The frequency of oscillation is found from (4.2-2) to be

$$f_0 = 1/(2\pi\sqrt{3}\ RC) \qquad (4.2\text{-}3)$$

Fig.4.9b depicts the phasor diagram obtained from the oscillator at different nodes. The signals V_1, V_2, and V_3 or V_0, V_0', and $-V_3$ form two sets of three-phase oscillation

signals. Also, all of these signals form a six-phase sequence.

4.2.0.2 Four-phase SD oscillator

Similarly, the four-phase oscillator is obtained using Tn, Tp and following the same technique described for the three-phase oscillator design. Y_1 and Y_2 are chosen as

$$Y_1 = G$$

$$Y_2 = jwC. \qquad (4.2\text{-}4)$$

The final circuit is shown in Fig.4.10a. The characteristic equation, assuming A1 = A2 = A , is given by

$$D(s) = (sRC)^2(-2A^2+2A-1)+2sRC(2A-1)+(-2A^2+2A-1) \qquad (4.2\text{-}5)$$

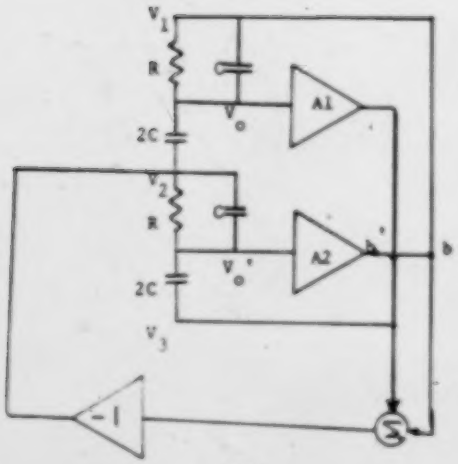
From (4.2-5), the condition of oscillation is satisfied when A=1/2. The corresponding frequency of oscillation is found to be

$$f_o = 1/(2\pi RC) \qquad (4.2\text{-}6)$$

The input and output sequence phase relationships as well as the oscillator network are given in Fig.4.10. Two sets of quadrature phase signals are available from the oscillator, namely, V_1, V_2, $-V_1$ and $-V_2$ as well as V_o,V_o', $-V_o$, and $-V_o'$. These two sets of signals are 45° out of phase, Fig.4.10b.

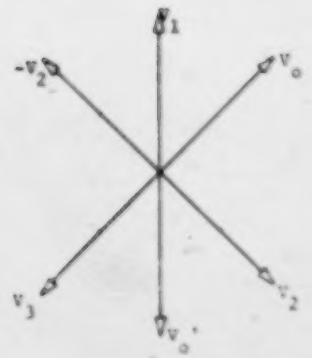
4.2.1 Switched-capacitor (SC) Multiphase Oscillators

Two classes of active RC oscillators can be used to derive the SC multiphase oscillator realizations. One is the SD oscillator while the other is the two-integrator-loop



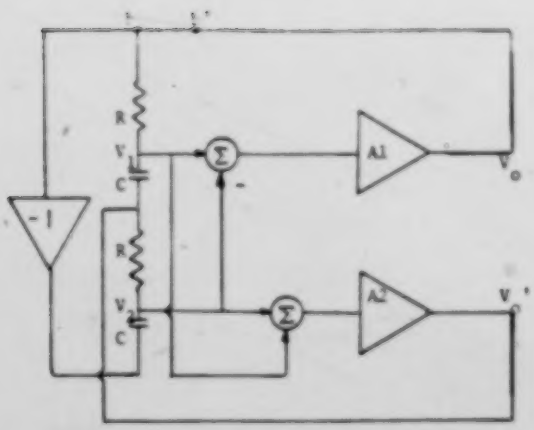
(a)

Fig. 4.9 (a) Three-phase and six-phase SD-Oscillators.



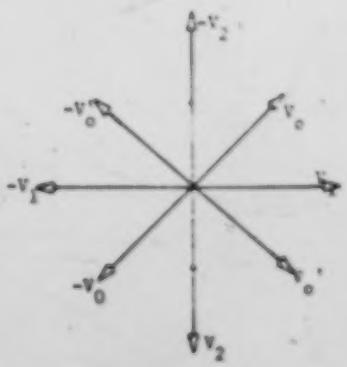
(b)

(b) Input and output sequences.



(a)

Fig. 4.10 (a) Fourphase SD Oscillator.



(b)

(b) Input and output sequences.

oscillator. The oscillator signals obtained from the SC oscillator are sampled-and-held sinusoids. The harmonics can be reduced by increasing the number of samples per oscillation cycle k. k is independent of the clock frequency fc but is related to a capacitor ratio in the oscillator circuit.

4.2.1.1 The switched-capacitor sequence discriminator oscillator

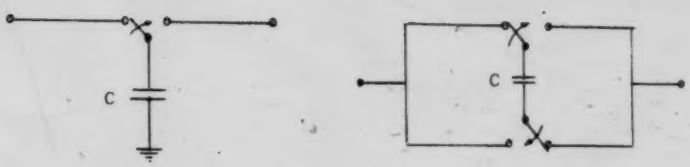
The SC version of the SD oscillator can be realized by replacing each resistor by the SC's. Two possible circuits can be adopted. Note that these realizations do not have the stray capacitance insensitivity as the loss-less discrete integrator (LDI) SCO's .

The SCO can be obtained when the basic SC's are employed (Fig.4.11). In this case, the jw axis in the s domain is not mapped into the unit circle in the z domain. Therefore, the feedback gain has to be adjusted in order to locate the poles on the unit circle. The frequency and gain of this realization can be derived from the charge conservation equation. (Appendix I). The corresponding feedback gain and frequency of oscillation of the four-phase oscillator are given as follows:

$$A = (1/\alpha)[-1+(\sqrt{2}/2)\sqrt{(\alpha+1)^2+1}], \qquad \alpha=C1/C \tag{4.2-7a}$$

$$f_o = (fc/2\pi)\arccos(\psi) = fc/k \tag{4.2-7b}$$

$$\psi = \frac{2\alpha^2+4\alpha+4+[(\sqrt{2}/2\alpha^2)\ -\sqrt{2}\alpha-2\sqrt{2}]\sqrt{(\alpha+1)^2+1}}{\alpha^4+2\alpha^3+4\alpha^2+4\alpha\ -(\sqrt{2}\alpha^2+\sqrt{2}\alpha+2\sqrt{2})\sqrt{(\alpha+1\ )^2+1}+4} \tag{4.2-8}$$



(a) (b)

Fig. 4.11 (a) The SC (b) The bilinear SC.

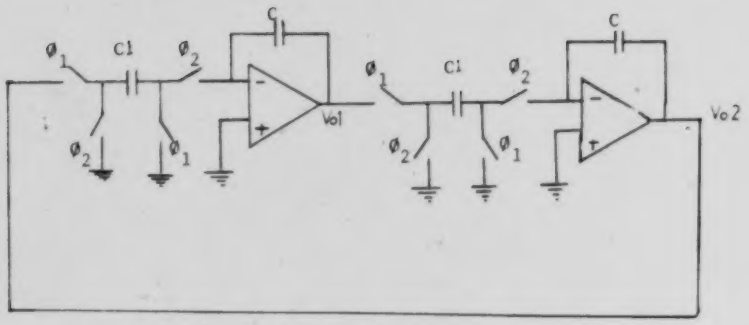
Again, for fixed C1 and C, f_o is directly proportional to fc. The ratio C1/C determines the number of samples in each oscillation cycle. The resulting circuit is bottom-plate stray insensitive. In most of the applications the capacitor ratio is chosen to be a fixed value and consequently the gain A is also fixed.

It is very interesting to note that the SCO's can generate sinewaves free from quantization error, for any value of k. A very wide range of k is realizable without increasing the complexity of the circuit of the SCO.

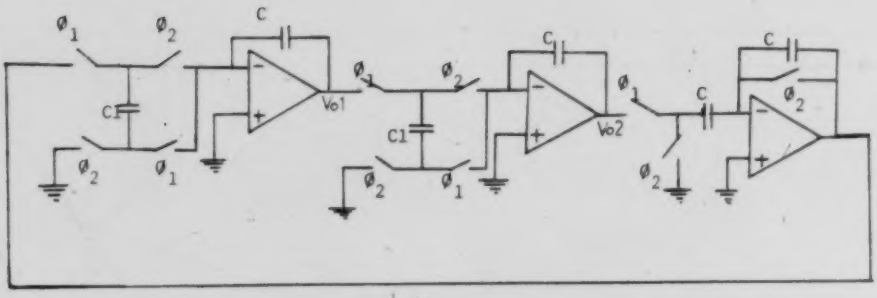
4.2.1.2 The Two-Integrator-Loop SCO

In principle it is possible to generate a harmonic signal by solving the corresponding differential equation by two successive integrations, and feeding the inverted resulting signal back to the input of the first integrator. The integrators can be of the form shown in Fig.3.1. By proper choice of the initial state of both integrators the required harmonic solution is obtained. Series connection of two of the SC integrators shown in Fig.3.4 results in Fig.4.12. In Fig.4.12 (a) and (b) the capacitor C1 and the four switches connected to the capacitor C1 are SC simulation of resistors.

However, these mathematical conditions are insufficient for the satisfactory operation of the real system. In the continuous two-integrator-loop oscillator, the phase differences after the second integration only approach 180°. Because of the inherent



(a)



(b)

Fig. 4.12(a) SCO using LDI's (b) SCO using BDI's

delay due to the sample/hold nature of switched capacitor circuits, two-integrator SCO's can obtain 180° phase shift. This is another virtue of SCO's.

The quadrature sine wave oscillators can be obtained based on the following system equations:

$$\dot{x} = w_o y$$

$$\dot{y} = -w_o x \qquad (4.2\text{-}9)$$

where x and y are the state variables.

To obtain the SCO realization, one can substitute the continuous integrator (Fig.3.1a) by a discrete integrator (Fig.3.4). The discrete integrator must have the transformation property such that the imaginary axis in the s plane maps to the unit circle in the z plane. Hence the well known loss less discrete integrator (LDI) and bilinear integrator are suitable for the realization. The oscillation frequency can be shown to be[43]

$$f_o = (fc/\pi)\text{arc Sin}(C1/2C), \qquad 2C>C1$$

$$= fc/k \qquad (4.2\text{-}10)$$

where C1 is the SC, fc is the sampling frequency which is equal to the clock frequency for the realization in Fig.4.12a, and k is the number of samples per oscillation cycle.

Using the bilinear discrete integrator (BDI), the frequency of oscillation is found to be

$$f_o = (fc/\pi)\text{arc tan}(C1/C)$$

$$= fc/k \qquad (4.2\text{-}11)$$

where C1 is the SC and fc is the sampling frequency which is equal to the clock frequency for the realization shown in Fig.4.12b.

From (4.2-10) and (4.2-11), for fixed capacitor ratios (C1/C), f_o is directly proportional to the clock frequency. The number of samples per cycle k versus the capacitor ratio C/C1 is shown in Fig.4.13. For a given k, the LDI realization uses less total capacitance. This is because for the minimum value C1, which is dictated by the MOS technology, the LDI requires a smaller value for C. In addition, the stray insensitive inverting and noninverting LDI circuits are available with relatively simple configurations. This allows the use of smaller capacitors in the LDI realization.

Switched capacitor techniques can be used to generate nonsinusoidal signals also. An almost sinusoidal signal can be shaped from the nonsinusoidal signal.

In the following the principle of untuned oscillators is described. Examples of RC untuned oscillators and SC untuned oscillators are given followed by a method of shaping sinusoidal waves from a square wave.

Untuned oscillators:

This class of oscillators have been widely integrated using bipolar technology. The basic operation of untuned oscillator is shown in the block diagram of

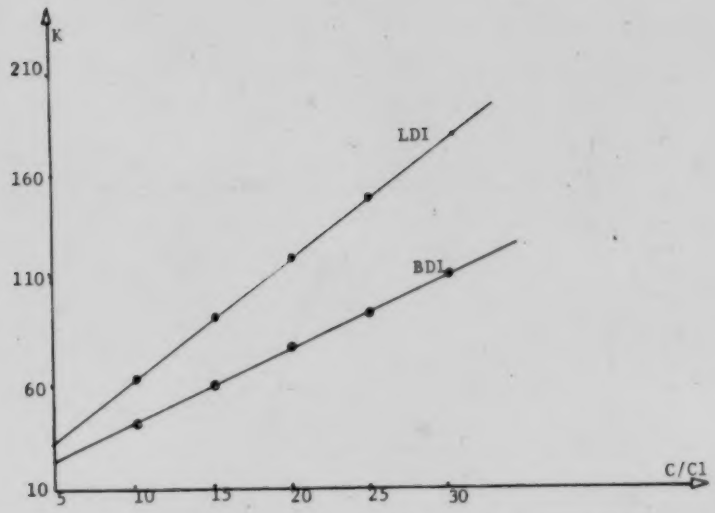


Fig. 4.13 The number of samples per cycle k versus the capacitor ratio C/Cl.

Fig.4.14. We see that all the components of this block diagram are compatible with the techniques we have studied in switched capacitor circuits. The untuned oscillator provides a square wave and a triangular wave. If a sinusoid is desired, then a circuit that converts the triangular waveform into a sinusoid is required. One possibility is to use the large signal characteristics of an MOS differential amplifier to approximate the triangle-to-sine conversion. The untuned oscillator has the advantage of not requiring a tuned circuit, so that the frequency can be easily controlled or varied. The amplitude is also well controlled and does not require a limiting circuit. The only disadvantage is that a sine wave is difficult to obtain.

Fig.4.15 shows a block diagram of the untuned oscillator and its principle of operation. We note that the basic ingredients of the untuned oscillator are an integrator and a bistable circuit. The operation of the untuned oscillator can be described as follows. During the time interval from 0 to T1, the integrator is integrating the voltage L_- provided by the bistable. If k is the constant of integration, we find that the value of VT at t= T1 is given as

$$VT(T1) = S_+ = kL_-T1+S_- \qquad (4.2\text{-}12)$$

where all these terms are defined in Fig.4.15. From eq.(4.2-12)

we get

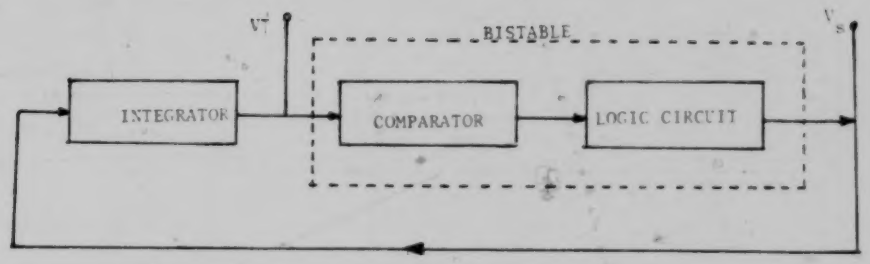
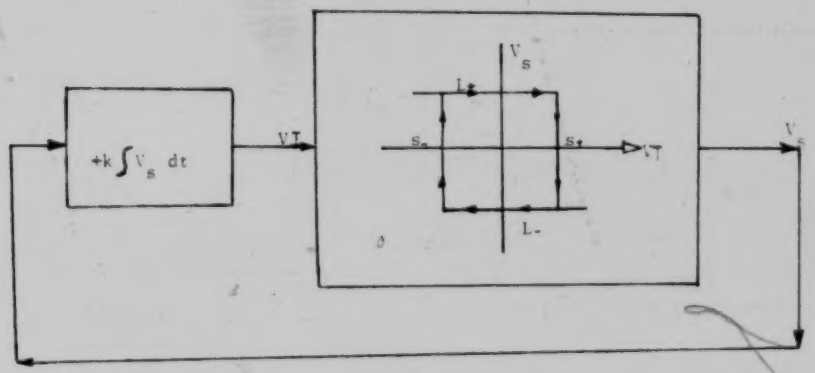


Fig. 4.14 Basic block diagram of an untuned oscillator



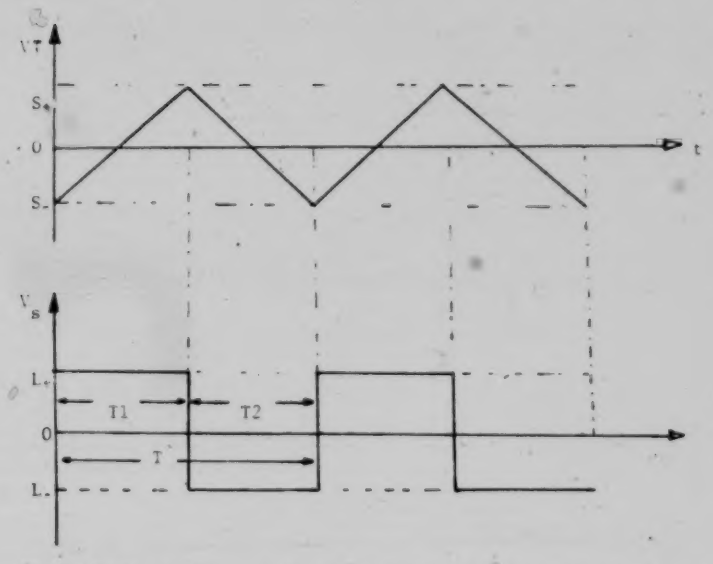


Fig. 4.15 Block diagram of the untuned oscillator and waveforms

$$T1 = (S_+ - S_-)/kL_+ \qquad (4.2\text{-}13)$$

We note that the integrator is a noninverting integrator. At t = T1, the bistable switches from L_+ at the output to L_-. Therefore during the time interval from T1 to T, the period of the oscillator, the integrator integrates L_-. Assume that t=T1=0 for the following analysis. At t = T2, the value of VT is given as

$$VT(T2) = S_- = kL_- T2 + S_+ \qquad (4.2\text{-}14)$$

From eq.(4.2-14), we can solve for T2 as

$$T2 = (S_- - S_+)/kL_- = -(S_+ - S_-)/kL_- \qquad (4.2\text{-}15)$$

Therefore, the period of the oscillator T can be written as

$$T = T1 + T2 = (1/k)\{[(S_+ - S_-)/L_+] - [(S_+ - S_-)/L_-]\} \qquad (4.2\text{-}16)$$

If $S_+ = -S_- = S$ and $L_+ = -L_- = L$, then eq.(4.2-16) reduces to

$$T = 4S/kL \qquad (4.2\text{-}17)$$

or the frequency of the untuned oscillator is

$$f_0 = kL/4S \qquad (4.2\text{-}18)$$

These results are general and may be used for all oscillators that fit the block diagram of Fig.4.15.

RC Untuned oscillator:

Fig.4.16 shows an analog untuned oscillator. If the op amps are powered from a positive voltage whose magnitude is Vps and a negative voltage whose magnitude is Vns, then it can be shown[1] that

$L_+ = Vps$, $L_- = -Vns$, $S_+ = Vps(R_3/(R_2+R_3))$, and

$S_- = -Vns\ (R_3 / (R_2+R_3))$. The constant of integration is $k=1/(R_1 C)$.

Assuming that the magnitude of Vps is equal to the magnitude of Vns, we find that the frequency of oscillation is

$$f_o = (1/4\ R_1 C)[R_3/(R_2+R_3)] \qquad (4.2\text{-}19)$$

S.C. Untuned oscillator:

An SC realization of Fig.4.16 is shown in Fig.4.17. The resistors R_2 and R_3 have been replaced by capacitors. This should cause no real problem, for this op amp is at either its positive limit or its negative limit.

Thus only one SC simulated resistor is needed. The frequency of oscillation for this circuit is

$$f_o = (C_1\ fc/4C)[C_2/(C_2+C_3)] \qquad (4.2\text{-}20)$$

A simpler version of this circuit is shown in Fig.4.18. It can be shown that the frequency of oscillation is given by

$$f_o = (C_1\ fc/2C)[Ln(1+\alpha/1-\alpha)] \qquad (4.2\text{-}21)$$

where

$$\alpha = C_2/(C_2+C_3) \qquad (4.2.22)$$

The above results assume that fc is much greater than f_o.

Shaping of sinewave from untuned oscillator:

Another method of generating a sinusoid is to divide down the clock frequency and to apply this square wave to a high Q band-pass network. Fig.4.19 shows a second-order bandpass filter that is used to convert a square wave into two sinusoids with a phase shift of 90° between them.

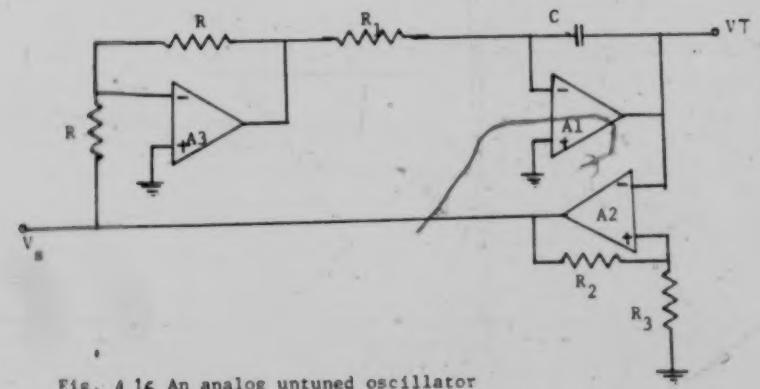


Fig. 4.16 An analog untuned oscillator

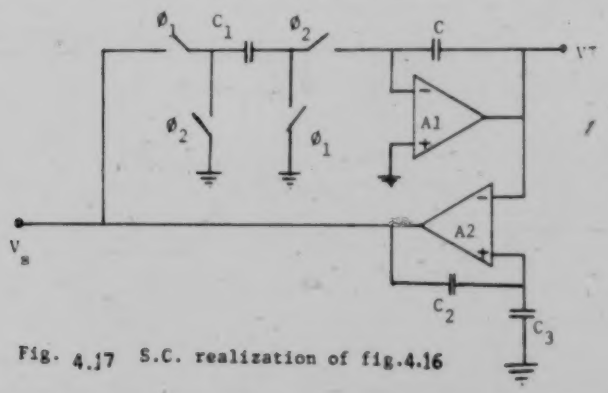


Fig. 4.17 S.C. realization of fig.4.16

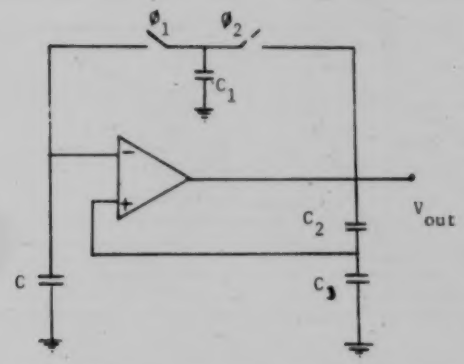


Fig.4.18 A simple one-amplifier oscillator

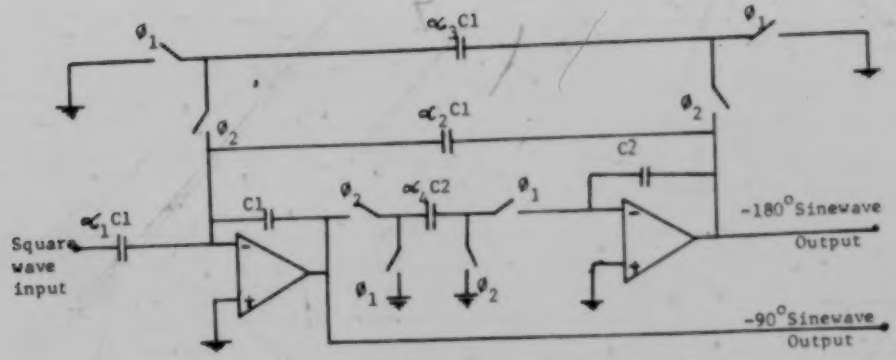


Fig. 4.19 A second order BPF used to convert a square wave into two sinusoids with 90° phase shift between them

Assuming that the square wave has a frequency of w_o and a zero-to-peak amplitude of Vsq, it can be shown that

$$\alpha_1 = (\pi/4)[Vsin/Vsq](1/Q) \qquad (4.2\text{-}23)$$

$$\alpha_2 = 1/Q \qquad (4.2\text{-}24)$$

and

$$\alpha_3 = \alpha_4 = 2Sin(w_oT/2) \qquad (4.2\text{-}25)$$

where Vsin is the zero-to-peak amplitude of the sine wave outputs. An interesting application of this circuit is to add weighted versions of the two outputs to get a low distortion sinusoid having any desired phase shift with respect to the square wave input.

4.3 Frequency stability of the SCO's

From (4.2-8) and (4.2-9), since k>>1, then for the SCO derived using the LDI transformation

$$f_o = fc/k \simeq (fc/\pi)(\alpha/2) \qquad (4.3\text{-}1)$$

where α=C1/C.

From (4.3-1), the SCO frequency depends on a capacitor ratio which can be realized with much better accuracy compared with absolute value accuracy. This is another important advantage over continuous type oscillators. Also from (4.2-8) and (4.2-9), it can be shown that

$$\Delta f_o/f_o \simeq \Delta\alpha/\alpha \qquad (4.3\text{-}2)$$

Thus the normalized change in the frequency of oscillation is also dependent on a normalized change in a capacitor ratio rather than absolute values. Very stable values of as small as 0.01 are realizable using current MOS technology.

Similarly from (4.3-1), the change in f_o due to the clock change is given by

$$\Delta f_o/f_o = \Delta fc/fc \qquad (4.3-3)$$

Since very stable clocks are achievable, then the change in f_o due to the clock frequency variations is negligible.

The effect of nonidealness of the op amps on the performance of the SCO can be investigated in two separate modes; namely, the small-signal and the large-signal modes of operation. In the small-signal analysis, the oscillator performance is influenced mainly by the finite op amp's gain-bandwidth products (GBWP). In the large-signal case, the oscillator performance will be altered by the nonlinear operation of the op amp's, namely, the finite slew rate.

Frequency Spectrum

Ideally, the frequency spectrum of the SCO output with zero-order hold can be expressed as

$$H(w) = [\partial(w-w_o)+\sum_{n=1}^{\infty}\partial(wc\pm w_o)](\text{Sin } w.tp/2)/(w.tp/2) \qquad (4.3-4)$$

For reasonable values of k, i.e., k>>1, an optional simple smoothing filter may be used to reduce the higher harmonics. For k>>1, the frequency spacing between the lowest harmonic at $fc-f_o$ and f_o is approximately fc. For k=50, as an example, the seperation is roughly five octaves. Consequently, a first-order RC filter can achieve about 40 dB of harmonics attenuation plus the attenuation by $(\text{Sin}\beta)/\beta$ effect (Fig.4.20). From(4.3-4), for a fixed k, the term

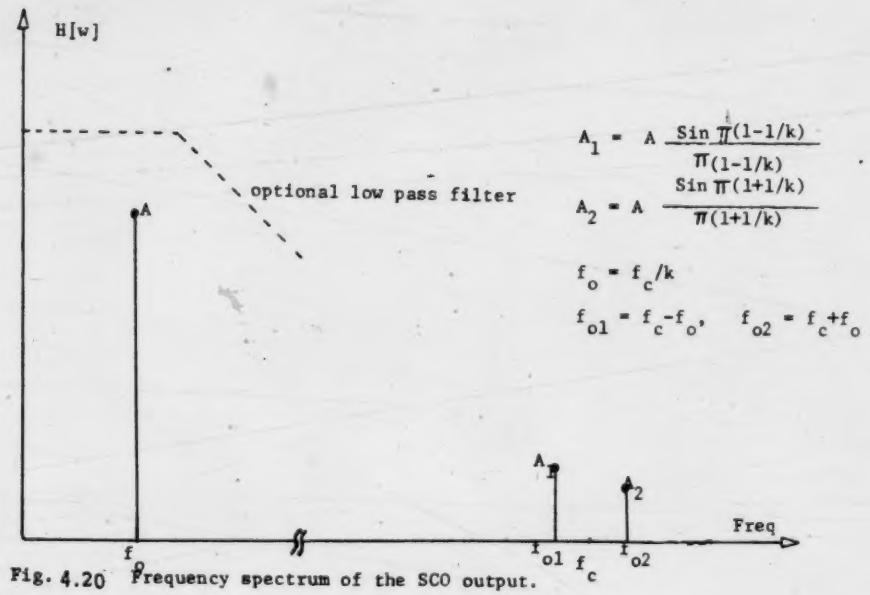


Fig. 4.20 Frequency spectrum of the SCO output.

$(\mathrm{Sin}\beta)/\beta$ is constant for any oscillation frequency f_o, independent of the clock frequency fc. So, the amplitude of the fundamental (or any specific harmonic) stays constant when the oscillation frequency is varied by changing the clock frequency.

5. AMPLITUDE CONTROL AND STABILIZATION OF OSCILLATORS

5.1 Introduction :

Amplitude stability is one of the main requirements associated with the design of oscillators. A practical sine-wave oscillator cannot be constructed entirely from linear elements, since some form of non-linearity is required to stabilize the output amplitude. This non-linearity usually contributes in some measure to harmonic distortion in the output waveform.

It is known from theory that an ideal sinusoidal oscillator has its poles on the jw-axis of the s-plane and thus exhibits an undistorted constant amplitude output. In a practical circuit, however, the poles are placed slightly in the right halfplane to ensure starting the oscillation. This means that the output will be bounded by an exponentially increasing envelope which continues to grow until limited by the output capability of the power amplifier. To prevent this from happening, some form of amplitude regulation is necessary.

There are mainly three ways of regulating the amplitude of oscillation.

1) through use of limiting circuits
2) through use of automatic gain control circuits
3) by the node voltage restoration method.

In the limiting type regulation, the amplitude is made slightly divergent, then the amplitude limiting is imposed

to keep the output bounded. The disadvantage of this method is the increased steady-state harmonic distortion as a result of amplitude limiting. To reduce the distortion, the AGC method can be employed where the output amplitude is detected and compared with a reference level. The resulting error signal is then used for automatic gain control to force the amplitude to converge to the specified level. In most circumstances this method requires a compromise to be made between harmonic distortion and the response time of the amplitude stabilization mechanism. In the restoration method the sample supplied from a reference circuit establishes the instantaneous value of voltage at the control node in the positive feedback two-port of the oscillators (this is done once in each period). In this method the problems of total harmonic distortion (THD) and amplitude transient are divided. THD depends on the circuit tuning whereas the speed of amplitude settling depends on the ability of Vref, the reference voltage, and the chosen circuit topology.

5.2 Limiting type amplitude stabilization

In the limiting method, control circuits monitor the instantaneous value of the output signal of the oscillator and introduce a nonlinearity into the maintaining amplifier when the amplitude exceeds a certain value. The effect of the nonlinearity is to momentarily reduce the gain of the amplifier with a subsequent stabilization of amplitude.

Practical realizations of this kind of gain control may use zener diodes, JFETS as voltage-controlled resistors, and other similar approaches. In most of these circuits the control mechanism may only be triggered in one half-cycle (positive or negative) of the output waveform so that there is a possibility of amplitude build up in the unmonitored half-cycle. This might cause distortions in the output and limit the use of the oscillator to general purpose applications. Another drawback for this type of amplitude regulation is that it normally does not prevent the amplitude from falling below the desired level if, for example, the amplifier parameters change. This kind of problem limits the temperature range in which the oscillator may operate properly. It is clear from the above discussion, therefore, that oscillators which use simple limiting-type amplitude regulation are adequate only in cases where amplitude stability and distortion requirements are not very critical.

5.2.1 Limiting type amplitude stabilization analysis

The oscillator with limiting type amplitude stabilization can be described[43] using the Van der Pol oscillator. The equations representing such an oscillator are given by

$$\dot{x}=w_o y$$

$$\dot{y}=-w_o x+\epsilon(1-\mu x^2)y \qquad (5.2\text{-}1)$$

$$=-w_o x+Ny$$

where x and y are the state variables, ϵ and μ are constants and, N represents the nonlinearity in the system.

The explicit expression for the first approximation of the Van der Pol oscillator (μ = 1) is given by

$$x = \frac{a_0 \exp(\epsilon t/2)}{\sqrt{1+(1/4)a_0^2[\exp(\epsilon t)-1]}} \quad \mathrm{Cos}(w_0 t+\theta) \qquad (5.2\text{-}2)$$

where a_0 is the initial value of the amplitude and θ is the phase angle (depending on the initial conditions).

The second approximation of (5.2-1) is

$$x=2\mathrm{Cos}(wt+\theta) - (\epsilon/4)\mathrm{Sin}\ 3(wt+\theta)$$

$$w=w_0(1-\epsilon^2/16). \qquad (5.2\text{-}3)$$

Note that, in contrast with the second approximation, the stationary state x is a pure sinusoidal oscillation in the first approximation (5.2-2). The amplitude and frequency in the steady state using the first approximation are

$$Vp=2/\sqrt{\mu}$$

$$f_0=w_0/2\pi \qquad (5.2\text{-}4)$$

As the order of the approximation increases above the frist, higher harmonic terms appear in the solution of (5.2-1), as seen in (5.2-3). In order to achieve low-harmonic distortion, ϵ must be chosen as small as possible. On the other hand, from (5.2-2) , smaller ϵ implies longer settling time.

An oscillation circuit which matches the Van der Pol equation can be constructed according to the block diagram shown in Fig.5.1. The nonlinearity contained in the circuit

is a saturation (compression) amplifier. The corresponding gain V_o/V_i can be chosen as

$$V_o/Vi = g = g_o(1-bV_o^2) \qquad (5.2\text{-}5)$$

The input-output relationship is plotted in Fig.5.2 using (5.2-5). Hence, the equations of the system in Fig.5.1 can be shown to be

$$\dot{x}=\sqrt{K_2K_3}\ y \qquad (5.2\text{-}6)$$

$$\dot{y}=-\sqrt{K_2K_3}\ x + (K_2g_o - K_1)\ \{1- [bx^2]/[1-(K_1/K_2g_o)]\ \}y$$

The method of amplitude stabilization by use of a saturation amplifier has long been in use and does not require further discussion.

5.3 AGC amplitude stabilization

Another method of achieving a high degree of amplitude stability is to include an Automatic Gain Control (AGC) loop from the output of the entire oscillator network to some control point of the maintaining amplifier. Any variation from the desired output value is sensed and amplified into an error signal whose size and polarity are such that the amplitude variation will be forced to zero by the feedback loop.

Some form of an a.c-to-d.c. converter is generally used with a voltage-controlled attenuator to regulate the output amplitude by adjusting a feedback gain within the oscillator. The problem in this case is to convert amplitude information instantaneously into a d.c.voltage. This d.c.

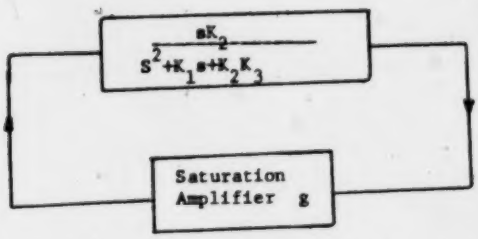


Fig.5.1 Block diagram of oscillator with limiting type amplitude stabilization.

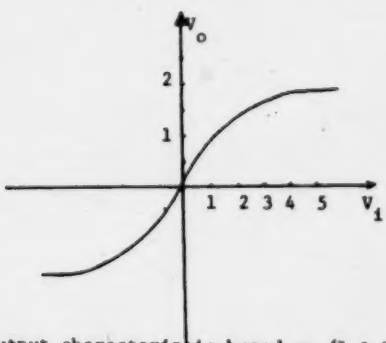


Fig. 5.2 Input-Output characteristic based on (5.2-5) (b=0.1., g_o=1).

voltage must have as little superimposed ripple as possible, since this ripple, when multiplied by a sinusoid at the fundamental frequency in the voltage-controlled attenuator, will introduce harmonic components into the oscillator output. A low-pass filter can be used following the rectifier, but this results in slower amplitude transient response. If the a.c.-to- d.c. converter is a simple half-wave rectifier, for instance, 0.1% distortion corresponds to an amplitude settling time of several hundred cycles.

One of the solutions is to replace the rectifier by a sample/hold which samples the oscillator output over some interval around its peak. The amplitude regulation system is then a hybrid of discrete-time and continuous-time elements which can be optimized by z-transform methods[59]. The effects of non-ideal behaviour in the sample/hold (such as finite sampling time and decay between samples) on harmonic distortion can be determined by Fourier analysis.

The amplitude control network, in general, should meet the following requirements:

1. Continuity of the amplitude versus control signal;
2. Ability to cover the desired amplitude range with a relatively small control signal range;
3. Almost zero hysteresis for the control curve;
4. The control signal should not load the oscillator.

5.3.1 Linear AGC Model for Oscillators

In oscillators there is no external input signal, and in practice there is no way of making measurements at the input of the maintaining amplifier without disturbing the oscillations. It may only be said that the "input", which is generated internally, is of the same form (shape and phase) as the output signal the only difference being the amplitude. A large and abrupt change in amplitude may be experienced during power turn-on, and care should be taken in the design of AGC loops for oscillators to make sure that they operate properly when power is turned-on. It is quite correct to assume that when an oscillator is set to operate at a certain point with some value of amplitude then small variations about the operating point occur. Obviously a large gain dynamic range for the AGC system is not necessary and a linear model representation of the gain control function is accurate enough[53].

A study of the stability problem of the AGC loop shows that an oscillator has an inherent property of an integrator, a fact which should be taken into account when designing the loop. The transfer function of the loop filter, the position of the filter in the loop and the components chosen for its design should be selected with care.

5.3.2 AGC type amplitude control analysis

AGC type amplitude control can be represented by the following state equations:

$$\dot{x} = w_o y$$

$$\dot{y} = -w_o x + \epsilon w_o (Vr - \mu Vp(t))y \qquad (5.3\text{-}1)$$

$$= -w_o x + w_o N y$$

where Vr is the reference voltage, Vp(t) is the peak voltage of the output, and ϵ and μ are constants.

The signal flow graph simulation corresponding to (5.3-1) is shown in Fig.5.3. Defining $Vr - \mu Vp(t) = Vc$, it is shown that the output peak Vp and Vc are related for small amplitude changes by

$$Vp(s) = Vc(s)[(\epsilon w_o Vp_o)/(2s)] \qquad (5.3\text{-}2)$$

where Vpo is the initial peak voltage. Then the control loop between the reference voltage Vr and the peak voltage Vp is shown in Fig.5.4. The solution of (5.3-1) can be approximated by

$$x(t) = Vp(t) \sin w_o t, \qquad (\mu = 1) \qquad (5.3\text{-}3)$$

Several methods have been adopted to obtain Vp(t). Three approaches are presented here.

The first method relies on the fact that the solution of (5.3-1) is approximated by

$x(t) = Vp(t) \sin w_o t$, and $y(t) = -Vp(t)\cos w_o t$. Hence, $Vp^2 = x^2 + y^2$ corresponds to the peak amplitude of the output. Substituting for Vp by $x^2 + y^2$ in (5.3-1), results in the improved Van der pol oscillator, proposed by Kaplan which is described by

Fig. 5.3 Signal flow graph of oscillator with AGC amplitude control.

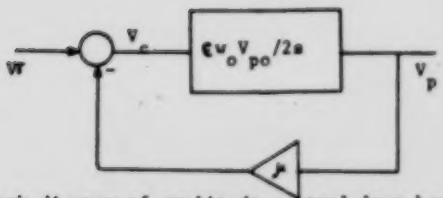


Fig. 5.4 Block diagram of amplitude control loop based on (5.3-1) and (5.3-2).

$$\dot{x} = wy$$

$$\dot{y} = -wx+\epsilon[1-\mu(x^2+y^2)]y \qquad (5.3\text{-}4)$$

Equation (5.3-4) can be written in the polar coordinates.

$$\dot{r} = \epsilon[1-\mu r^2]r\,\mathrm{Sin}^2\theta$$

$$\dot{\theta} = -w - \epsilon[1-\mu r^2]\,\mathrm{Cos}\theta\,\mathrm{Sin}\theta \qquad (5.3\text{-}5)$$

Rewriting (5.3-5) in a slightly different form

$$\dot{r} = \epsilon[1-\mu r^2]r[(1/2) - (\mathrm{Cos}2\theta / 2)]$$

$$\dot{\theta} = -w-\epsilon[1-\mu r^2](1/2)\mathrm{Sin}\,2\theta. \qquad (5.3\text{-}6)$$

Using the principle of averaging, since the mean values of $(\cos 2\theta)$ and $(\sin 2\theta)$ are equal to zero, (5.3-6) can be approximated by

$$\dot{r} \simeq \dot{r}_1 = (\epsilon/2)[1-\mu r^2]r$$

$$\dot{\theta} \simeq \dot{\theta}_1 = -w \qquad (5.3\text{-}7)$$

The solution of (5.3-4) can be approximated by solving (5.3-7) which yields

$$x = (\mathrm{Cos}\ wt) \,/\, \{\sqrt{\mu[1 - h\ \exp(-\epsilon t\ )]}\} \qquad (5.3\text{-}8)$$

where $h=1-(1/\mu Vp_o^2)$, Vp_o is the initial peak.

The generation of Vp^2 requires both squaring and summing operations. The analog squarer can be realized using relatively simple circuitry. The variable gain N can be realized using the analog multiplier.

In the second method Vp is obtained using a rectifier followed by a low-pass filter (LPF). In this case, the control block diagram should include the LPF as shown in Fig.5.5. Referring to Fig.5.5, which assumes a first-order LPF, the closed loop transfer function can be shown to be

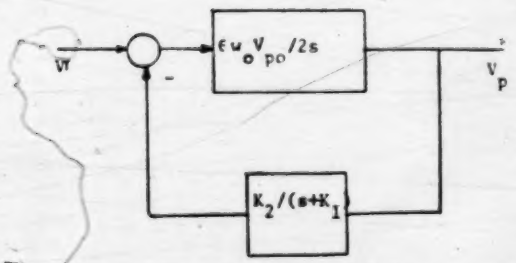


Fig. 5.5 Block diagram of amplitude control loop containing LPF.

$$\frac{Vp}{Vr} = \frac{(\epsilon w_o Vp_o/2)(s+k_1)}{s^2 + k_1 s + (k_2 \epsilon w_o\ Vp_o)/2} \qquad (5.3\text{-}9)$$

k_1, k_2, and ϵ are design parameters which have to be to be chosen carefully since they determine the transient and the steady-state behavior of the control loop. Also, the LPF has to reject most of the harmonics introduced by the rectifier. Otherwise, the superimposed ripples on the control signal Vc will cause harmonic distortion. The introduction of low-pass filtering in the control loop tends to extend the settling time.

The third method employs the sample and hold technique, where the oscillator output is sampled around the peak. This sample-and-held signal is the peak voltage Vp sampled-and-held with a sampling period which is equal to the oscillation period. Although there is no steady-state error in Vp(t) in this method, a limit on ϵ has to be imposed to insure the stability of the control loop.

From Fig.5.6, the closed-loop gain of the control loop is obtained as

$$H(z) = (\epsilon\pi Vp_o)/(z-1+\epsilon\pi Vp_o) \qquad (5.3\text{-}10)$$

To satisfy the stability criteria ϵ should be

$$0<\epsilon<(2/\pi Vp_o) \qquad (5.3\text{-}11)$$

The optimum choice of ϵ for the fastest settling is given by

$$\epsilon = 1/(\pi\ Vp_o).$$

$$\text{This results in } H(z) = 1/z \qquad (5.3\text{-}12)$$

From (5.3-12), it is seen that the oscillator output amplitude settles in one oscillation cycle only, for any

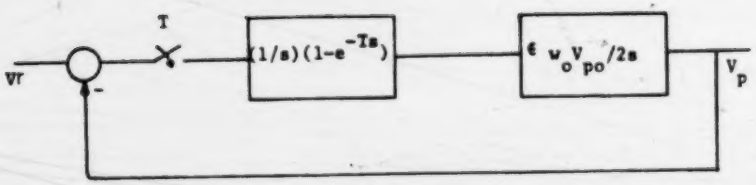


Fig. 5.6 Block diagram of amplitude control loop containing S/H .

form of incremental change in Vr.

Replacing the fixed amplifier gain a with the variable gain $e(Vr-\mu Vp(t))-1$, the AGC type amplitude control can be incorporated in the linear oscillators. The realization of such an amplifier is given in Fig.5.7 where an analog multiplier is employed to realize the variable gain amplifier.

In the discrete system, the described methods are also applicable. By examining the system equations (5.2-1) and (5.3-1), it is seen that these systems are composed of a conservative oscillator and a control term (Ny). This added control term brings the conservative system into a limit cycle. In the discrete design if the linear discrete part remains conservative (poles on the unit circle) and the control law stays the same, then the limit cycle should exist. There is no need to distinguish between a continuous and a discrete system in this case because the added control forces the amplitude of any conservative oscillator to converge to a specific level.

5.3.3 Example of AGC type control

The FET-stabilized Wien-bridge oscillator is well known. A low-distortion version, which can be used as a signal source in a precision capacitance measuring bridge is described[58].

A linear model is developed for the control loop, from which the small-signal behavior of the control loop can be

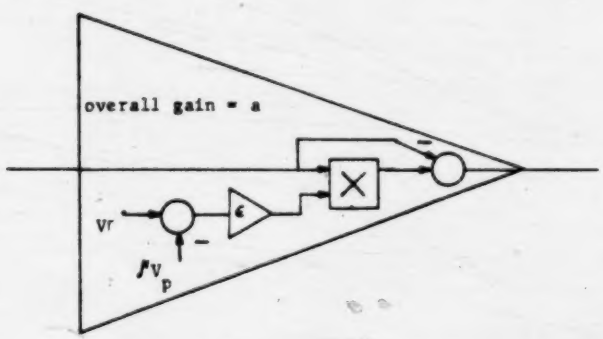


Fig. 5.7 Variable gain amplifier used in SD Oscillator amplitude control.

predicted. This leads to design equations for the amplitude-stabilizing loop.

Circuit Diagram:

The circuit diagram of the oscillator with its amplitude stabilizing loop is shown in Fig.5.8. The output voltage of the Wien-bridge oscillator is fed to a full-wave rectifier. The difference between the output voltage of the rectifier and the reference voltage Vref is integrated and filtered to obtain a d.c. control voltage at the gate of the FET, which controls the a.c. drain-source resistance of the FET in such a way that the output voltage of the oscillator is maintained at a constant amplitude.

The oscillator oscillates at a frequency

$$f = 1/(2\pi RC). \qquad (5.3\text{-}13a)$$

In a stable loop the integrator forces the difference between Vref and the mean value of the rectified output voltage of the oscillator to zero, thus maintaining the amplitude of oscillation at a precise value.

With V_o denoting the peak value of the output voltage, and assuming that the components are ideal, the mean value of the output voltage of the rectifier will be V_o/π, which leads to the conclusion that

$$V_o = \pi Vref. \qquad (5.3\text{-}13b)$$

The design considerations for this kind of control loop depend on whether the oscillator is designed for low distortion, or fast dynamic response. In the case of low distortion, care must be taken to ensure that the harmonic

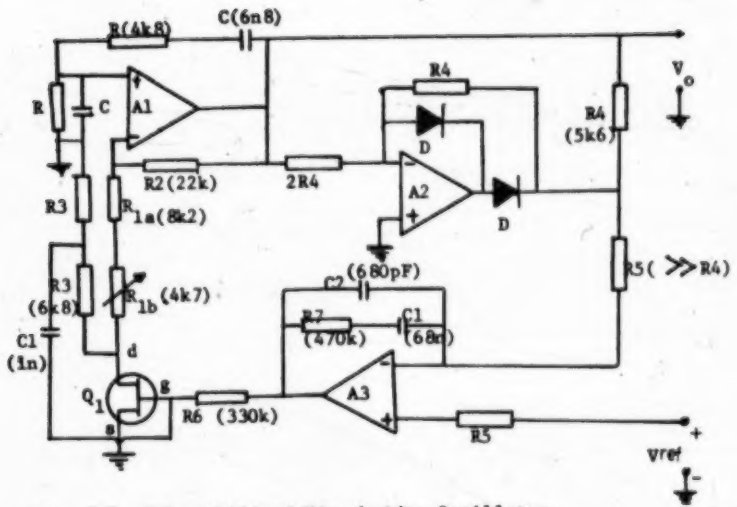


Fig. 5.8 FET stabilized Wien-bridge Oscillator.

components in the output signal of the rectifier (the first of which lies at twice the oscillator frequency) are highly attenuated at the gate of the FET.

5.4 Fast Amplitude Control

As stated before a stable sine wave oscillator cannot be constructed entirely from linear elements, since total linearity would leave the output amplitude indeterminate. We use this fact to our benefit and establish the oscillation amplitude restoring initial conditions at an arbitrary node in the oscillator. This restoration is done at least once in each oscillation period.

The circuit of fast amplitude control is shown in Fig.5.9. It includes comparators T1,T2,T3, and AND gate G1 which controls the switch S1 and a source of reference Vref. The circuit is connected to two nodes of oscillator, the synchronizing node "s" and the restoring node "r". The circuit operation can be analyzed using the steady state operation waveforms shown in Fig.5.10. T1 and T2 are connected as a window comparator thus $V\delta_1>0$, $V\delta_2<0$ and $|V\delta_1|$, $|V\delta_2|$ are small. The gate G1 produces a positive pulse Vg1 when the synchronizing voltage vs becomes zero and the restoring voltage is positive (we assume that the phase shift between these two voltages is less than 180°). At this instant the control circuit interferes with the oscillator for a very short period of time. It closes momentarily the switch S1 and the voltage vr becomes instantly equal to

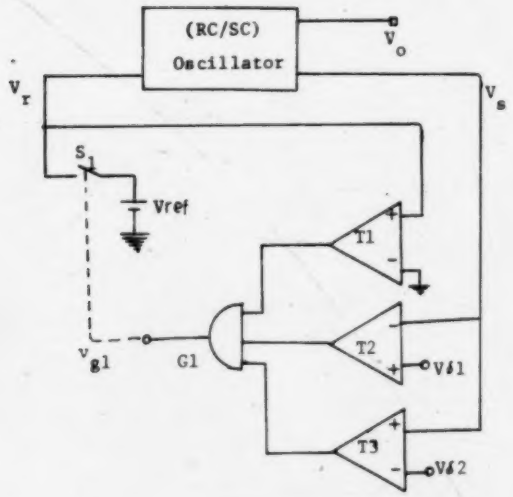


Fig.5.9 Fast amplitude control circuit.

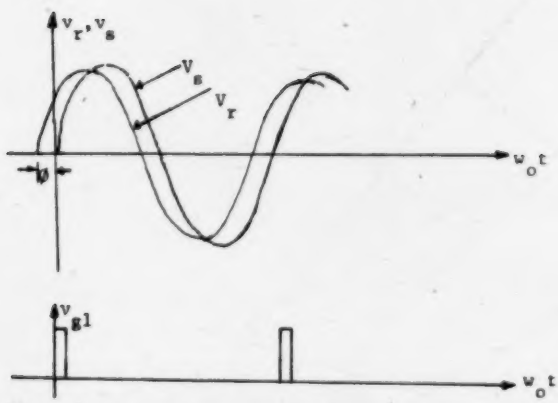


Fig. 5.10 Waveforms used to analyze fast amplitude control circuit.

Vref.

In the steady state oscillations

$$vs = Vsm \, Sin \, w_o t \qquad (5.4\text{-}1)$$

and

$$vr = Vrm \, Sin(w_o t + \phi) \qquad (5.4\text{-}2)$$

where w_o is the oscillation frequency depending on the oscillator circuit.

The oscillation amplitude at the restoring node is determined by the condition

$$Vrm \, Sin\phi = Vref \qquad (5.4\text{-}3)$$

The relationship between the amplitude Vom of the output voltage v_o and Vrm is established from the differential equation relating v_o to Vr or via the partial transfer function between the output node and restoring node.

If we change the reference voltage by a step the new value of Vom is established without any amplitude transient. The delay which is equal to one oscillation period is possible. (This is experimentally verified).

5.4.1 Exclusive SC method of amplitude stabilization

Another method [1] of limiting the amplitude using only SC elements is shown in Fig.5.11. This method rectifies and integrates the output to get a DC voltage that is proportional to the amplitude of the output sinusoid. This DC voltage is applied to the gate of an MOS device (M1) which is in series with a resistor to form RB. The gain of the integrator can be adjusted to vary the amplitude of the

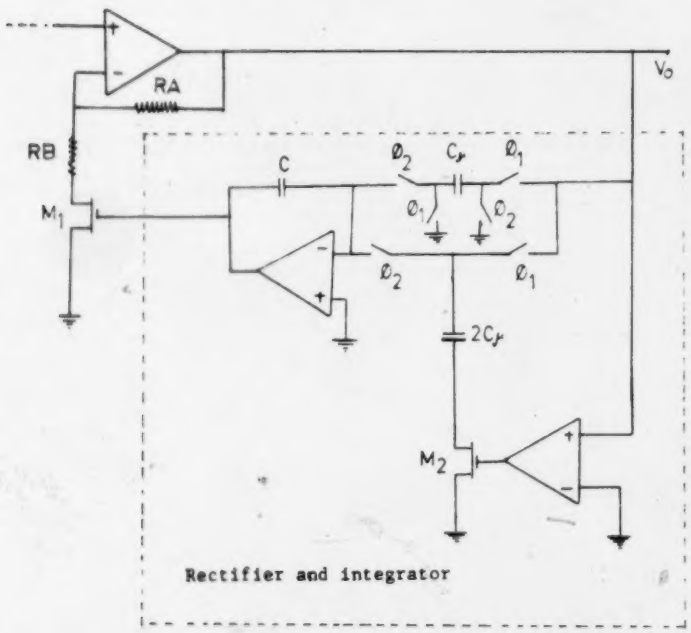


Fig.5.11 SC amplitude limiting circuit for oscillators

oscillator. This circuit depicts the fast integration achievable in SC techniques.

6. EXPERIMENTAL RESULTS

Experiments were conducted on some of the circuits discussed in the previous chapters. Importance was given to experiments using the fast amplitude control circuit on the Wein-bridge and twin-T bridge oscillators. As a result of the experiments, we observed that the fast amplitude control circuit achieves control in one period (a few periods in the twin-T) and also low distortions simultaneously.

Circuit operation

Twin-T oscillator:

The circuit of Fig.6.1 was based on the twin-T bridge shown in Fig.4.3. The resistors R_1,R_2, and R_3 are realized with the switched capacitors CR_1,CR_2, and CR_3. The amplitude regulation system was based on the circuit of Fig.5.9. The comparators T_2 and T_3 are used for the zero detection of the output amplitude v_o of the oscillator circuit. The switch 'S' is used to initialize the voltage on the capacitor C_3 once in each period of oscillation.

Wien-bridge oscillator:

The circuit of Fig.6.2 was based on the Wien-bridge oscillator shown in Fig.4.1. The resistors 'R' are realized with the switched capacitors 'CR'. The amplitude regulating system was based on the circuit of Fig.5.9 the same as for the twin-T. But here the node voltage restoration circuit is connected to the node Va restoring initial conditions on the capacitor C.

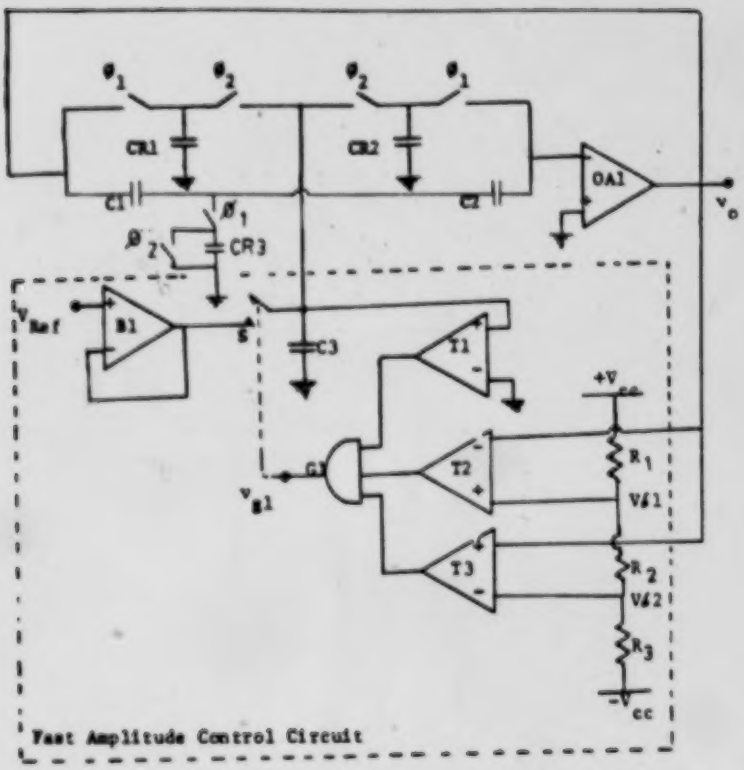


Fig. 6.1 Practical twin-T Oscillator with amplitude control.

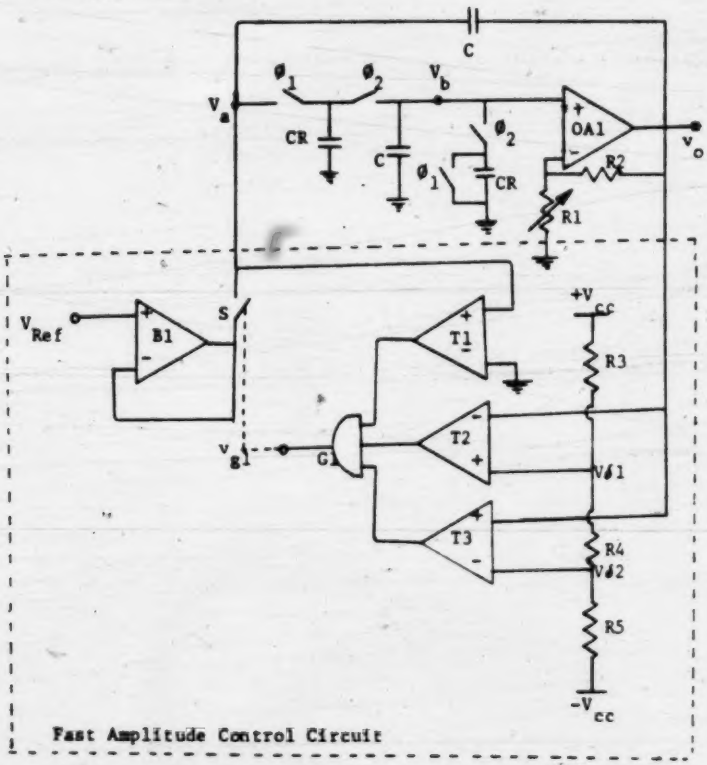


Fig. 6.2 Practical Wien-Bridge Oscillator with Amplitude Control.

Circuit specifications

Twin-T oscillator:

The twin-T oscillator shown in Fig.6.1 is designed to oscillate at 1.5 kHz with the component values as follows. $CR_1=CR_2=$ 1nF; $CR_3=$ 2nF; $C_1=C_2=$ 33nF; C_3 =66nF; $R_1=R_3=$ 10k; $R_2=$ 262Ω.

Op Amps are μA 741's; Comparators are LM 311's and MC 14012 is used for the gate. The switches are realized with MC 14066 CMOS Switches. The switches were operated using a 300 kHz non overlapping clock.

The output voltage waveforms when the amplitude control circuit is connected and disconnected are shown in Fig.6.3.

The Wien-bridge oscillator and two integrator loop oscillator were also realized experimentally and the respective output waveforms are shown in Fig.6.4 and 6.5.

Wien-bridge oscillor:

The Wien-bridge oscillator (Fig.6.2) was designed to oscillate at 5 kHz with the component values as follows.

CR=3.3 nF; C= 22nF; $R_2=$ 12k. A 10k potentiometer is used for R_1. $R_3=R_5=$ 10k; $R_4=$ 262Ω. Op Amps and comparators are realized with μA 741 and LM 311 respectively. MC 14012 is used for the gate G_1 and MC 14066 CMOS switches are used to simulate the switched capacitor resistors. A non overlapping clock of 200 kHz with 50% duty cycle was used for the switches.

The output voltage waveforms at two different reference voltages are shown in Fig.6.4(a) and (b).

Amplitude transient

To prove that these amplitude control circuits are indeed fast, we applied a rectangular voltage waveform of low frequency to the reference voltage terminal. The resulting output amplitude changes for twin-T oscillator and Wien-bridge oscillator are shown in Fig.6.6 and Fig.6.7 respectively. It is seen that the amplitude change occurs within one period of oscillation for Wien-bridge oscillator and three periods for twin-T oscillator. It can be shown[13] that by controlling the amplitude in both the half-periods of oscillation, the amplitude control can be achieved in one half-period of oscillation for Wien-bridge oscillator and with comparable speed for twin-T oscillator. This is indeed instantaneous control over the amplitude.

Stability of oscillator amplitude

The stability of these sinusoidal oscillators is checked by varying the power supply of the oscillator circuit over a wide range. It is found that there is no significant variation of the amplitude of the oscillator over the range of allowable minimum and maximum voltages of the op amps. When the power supply voltage is brought down to the minimum value essential for proper operation of the Op Amps, distortions in the oscillator amplitude are observed.

Total Harmonic Distortion

The width of the control pulse which is applied at a node of the oscillator circuit is varied and the resulting

waveforms are shown in Figs.6.8 and 6.9. To minimize distortions (see Fig.6.9) the control pulse width must be narrow. In Fig.6.8 there is no apparent distortion because the control pulse duration is about one clock cycle. In Fig.6.9 however the control pulse duration is several clock cycles resulting in a slightly distorted oscillator output. The control pulse width is varied by varying the resistor R_2 (Fig.6.1 while R_4 in Fig.6.2). The plots showing the %THD variation due to variation of control pulse duration are shown in Fig.6.10.

One of the differences in the harmonic content of RC oscillators and SC oscillators is that the SC oscillators have the harmonic contributions of the clock signal. When the frequency of oscillations is not far below the clock frequency, the total harmonic distortion becomes significant.

In the experimental measurement of THD, we used clock frequencies that are far above the frequency range measurable by the wave analyzer used. It can be deduced, therefore, that the measurement of THD in our experiments is identical to the measurement of THD of a continuous oscillator.

In the figures showing output oscillations, spikes can be observed. These spikes are due to the sampled data nature of the SC technique. The spikes which are essentially due to the clock can be removed by connecting a low pass filter at the output node of the oscillator. There are other possible

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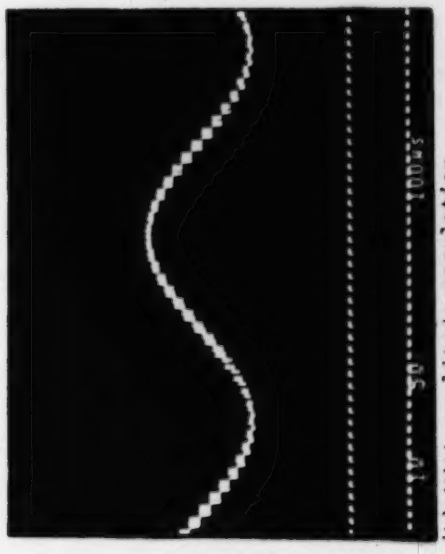
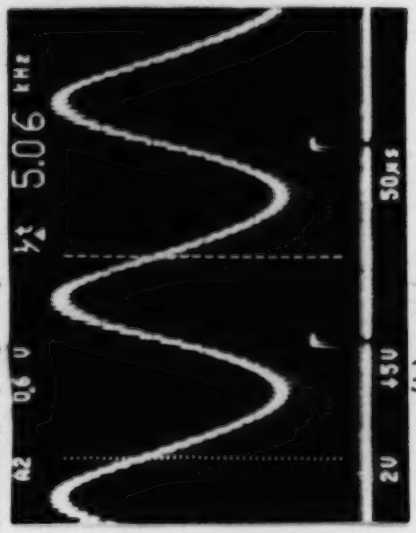


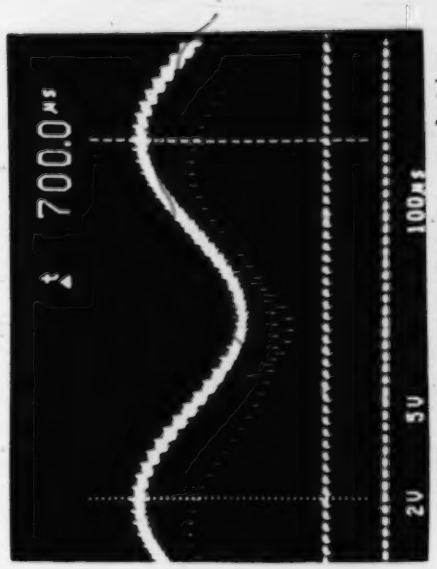
(b) With amplitude regulation

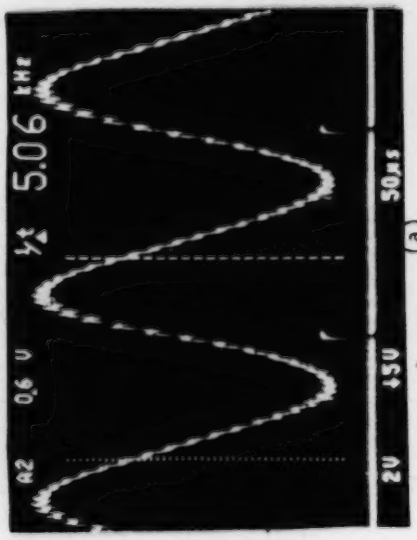
(a) Without amplitude regulation

Fig. 6.3 Out put waveforms of Twin-T Oscillator (Fig.6.1)



(b)





(a)

Fig.6.4 Output of Wien-bridge oscillator (Fig.6.2) at two different amplitudes.

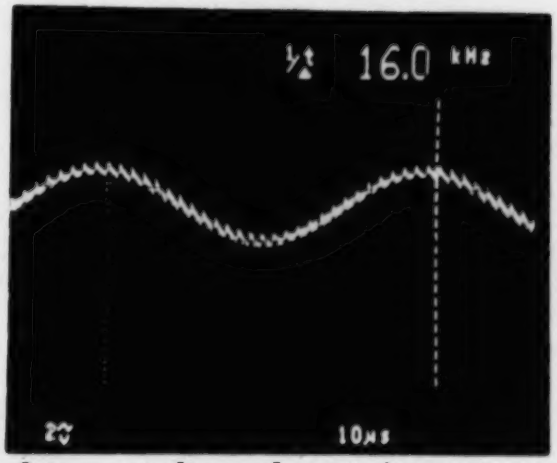
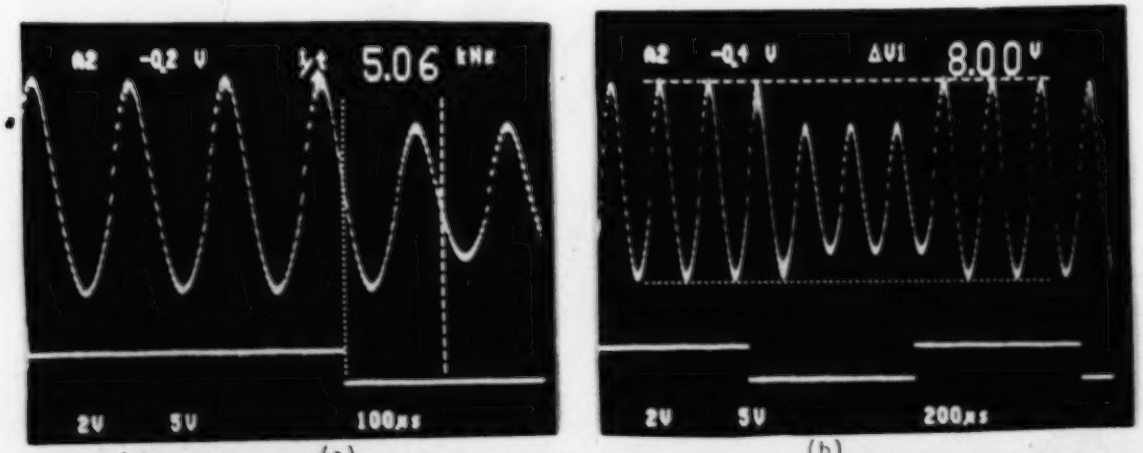


Fig. 6.5 Output waveforms of a two integrator oscillator.

Fig. 6.6 Twin-T Oscillator with reference voltage modulation



(a) (b)

Fig.6.7 Wien-bridge oscillator with reference voltage modulation.

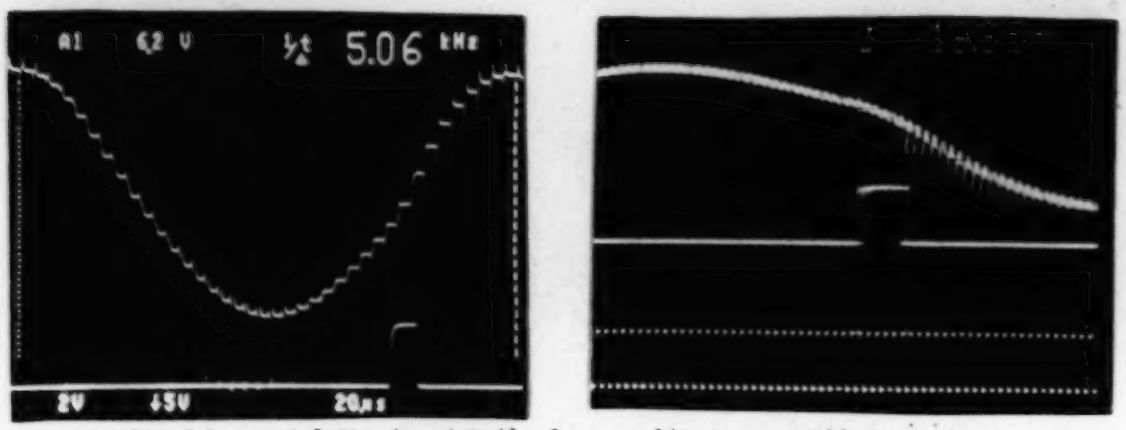


Fig.6.8 and 6.9 Showing detail of an amplitude controlled waveform with a narrow and a wide control pulse.

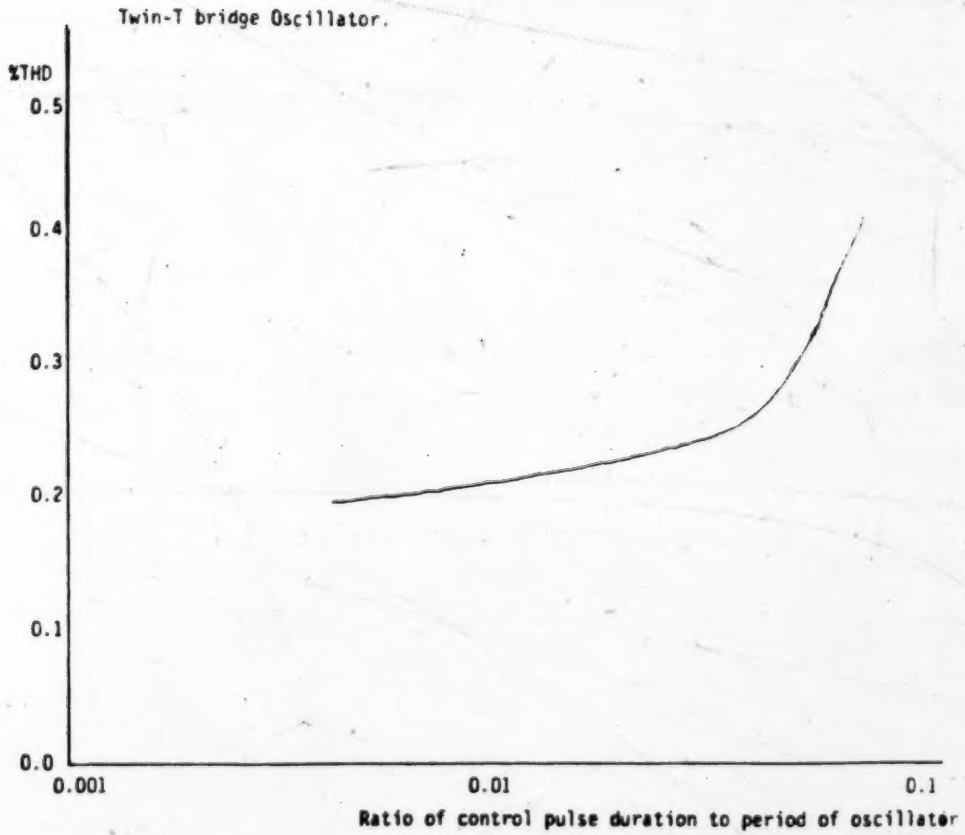


Fig.6.10a Distortion versus ratio of control pulse duration to period of oscillator.

Wien-bridge oscillator

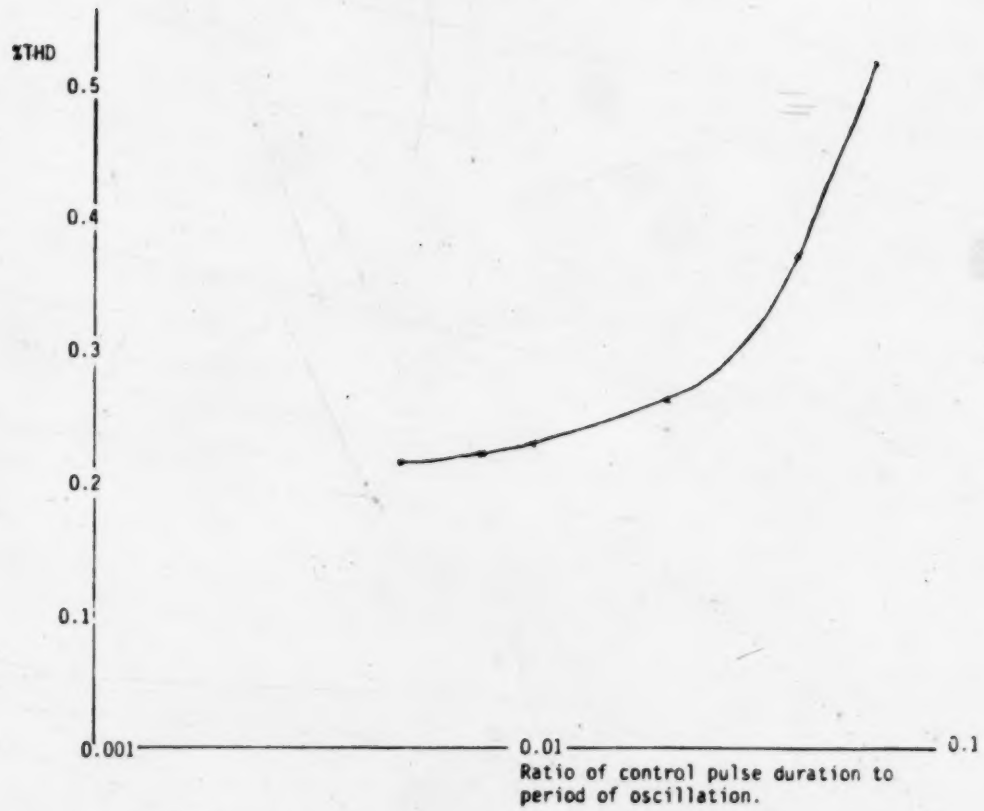
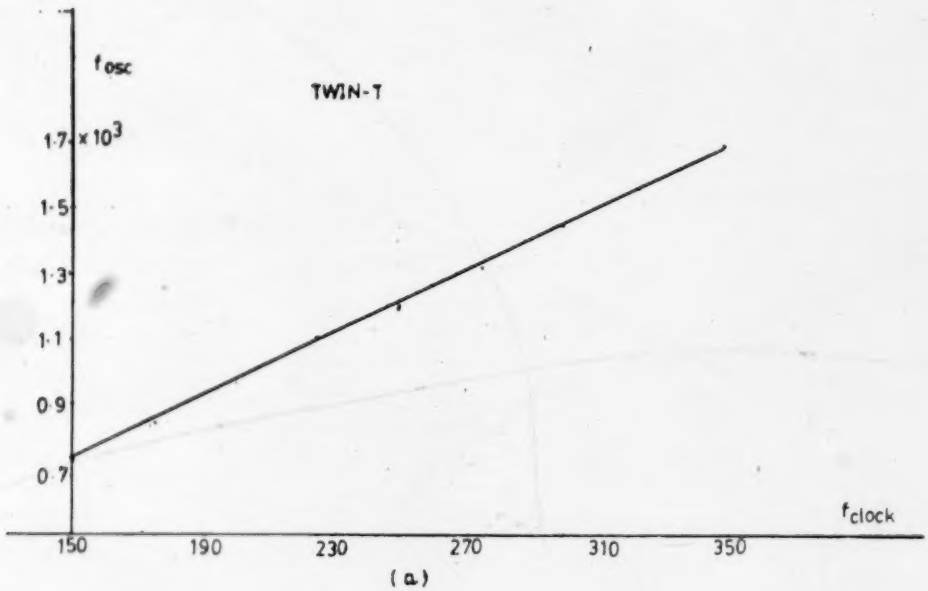


Fig.6.10b. Distortion versus ratio of control pulse duration to oscillation period.

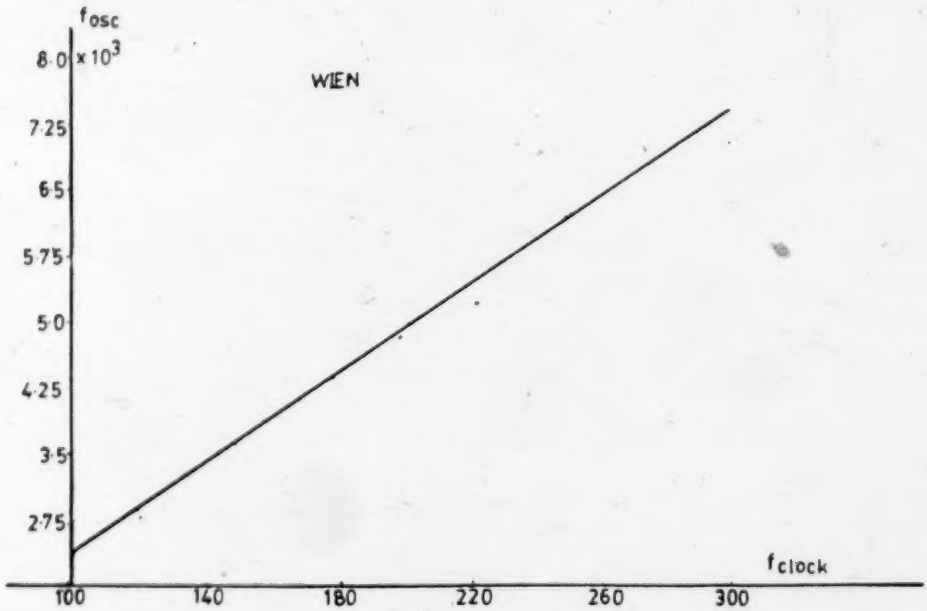
causes for the appearance of spikes. One such possibility is failure of break-before-make arrangement of switching. This problem can be solved by using clock duty-cycle slightly lessthan 50%.

Change of oscillation frequency

For both twin-T and Wien-bridge oscillators, the clock frequency is varied over a 200kHz range and the resulting oscillation frequency variations are plotted in the Fig.6.11 (a) and (b) respectively. The plots showing oscillation frequency versus clock frequency depict the linear variation of fosc versus fclock as expected theoretically for both twin-T and Wien-bridge oscillators. Over the range of oscillation frequency variation verified with clock frequency changing, no amplitude variation was observed.



(a)



(b)

Fig.6.11 a & b. Oscillation frequency versus clock frequency of Twin-T and Wien Oscillators respectively.

7. CONCLUSIONS AND RECOMMENDATIONS

The utilization of the switched-capacitor (SC) approach in the oscillator design provides many attractive and unique features. For example, the oscillation frequency is directly proportional to the clock repetition rate. Thus there is no need to change the oscillator elements to vary the oscillation frequency over a very wide range.

It is possible to develop fast settling RC/SC oscillators and to achieve low distortion figures simultaneously. The solution of this problem is found designing the circuits of amplitude control which restore a chosen node voltage (in the general case it can be a set of nodes) at least once in each oscillation period. By controlling the amplitude in both half-cycles of the oscillation, the amplitude control can be achieved in one half cycle of the oscillator[13].

Most methods of amplitude control require floating rectifiers and thus are not compatible for MOS realization. Thus, because the method of fast amplitude control by node restoration does not use floating rectifiers, it can be realized in MOS technologies as well as bipolar ones.

In the case of dual feedback, the negative feedback is minimum at the notch frequency, and the R2/R1 ratio (Fig.4.8c) is chosen so that positive feedback slightly exceeds the negative feedback at this frequency. Oscillation will occur at the notch frequency of the twin-T network.

It may be premised that the noise can be lower when realized on a chip rather than a breadboard. This conclusion is drawn from observing the better results obtained when the switching circuit was built on a PCB than on a breadboard. This is particularly true when the complexity of the SC resistor circuit increases, since the disturbances in the operation of the circuit were also found to increase.

One feature of the SC oscillators not discussed in detail in this dissertation is the clock feed-through. Due to the parasitic capacitances the voltages applied to the gates of the switches interfere with the circuit operation. One method of reducing this problem is illustrated in Fig.2.4.

In the practical circuits two switches were shown to realize a switched capacitor resistor. Realizations using more than two switches were also verified experimentally. The choice of switched capacitor resistors must be made considering the factors outlined in chapters 2 and 3.

The application of multiphase switched capacitors and programmable[2],[26] switched capacitors appears to be a potential research area. There is also a great need to develop analysis methods for circuits which include both continuous and switched capacitor elements. We believe that realizations which make use of the advantages of switched capacitor techniques combined with continuous circuits will result in better performance than exclusive switched capacitor realizations.

An amplitude modulated sine wave oscillator can be readily implemented by modulating the voltage Vref with the modulating signal. A capacitance to frequency converter for transducer applications can be realized by replacing any of the frequency determining capacitors by the variable capacitor. Frequency shiftkeying can be achieved by switching the resonant frequency determining capacitors in and out of the oscillator at the appropriate instants of time. By extending the switched-capacitor circuits capability into the megahertz range, a number of very attractive new applications, including video signal processing and IF filtering in communication systems, become feasible.

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9. APPENDIX

9.1 APPENDIX I

Derivations of gain and frequency of SCO using sequence discriminator

From Fig.A.I.1, the z-transformed charge conservation equations are given by

$$V_1(C_1+C-C/z)+V_4(-C+C/z)-Vb\ C_1/z = 0 \qquad (A.I-1)$$

$$V_2(C+C_1-C/z)+Vb(C-C/z)-V_4C_1/z = 0 \qquad (A.I-2)$$

let $\alpha = C_1/C$

$$V_1(\alpha+1-1/z)+V_4(-1+1/z)-Vb\ \alpha/z = 0 \qquad (A.I-3)$$

$$V_2(\alpha+1-1/z)+V_4\ \alpha/z+Vb(1-1/z) = 0 \qquad (A.I-4)$$

and

$$V_3 = (V_1-V_2)A \qquad (A.I-5)$$

$$V_4 = (V_1+V_2)A \qquad (A.I-6)$$

Substituting from (A.I-6) in (A.I-3) and (A.I-4), yeilds

$$V_1[\alpha+1-A+(A-1)/z]+V_2(A/z-A)-Vb\ \alpha/z = 0 \qquad (A.I-7)$$

$$V_1(-A\alpha/z)+V_2[\alpha+1-(A\alpha+1)/z]+Vb(1-1/z) = 0 \qquad (A.I-8)$$

solving for V_1 and V_2 from (A.I-7) and (A.I-8) yields

$$V_1 = \frac{(A/z-A)(1-1/z)+[1+\alpha-(A\alpha+1)/z]\alpha/z}{[\alpha+1-A+(A-1)/z][\alpha+1-(A\alpha+1)/z]+(A/z-A)A\alpha/z}\,Vb \qquad (A.I-9)$$

$$V_2 = \frac{(\alpha/z)(A\alpha/z)+(1/z-1)[\alpha+1-A+(A-1)/z]}{[\alpha+1-A+(A-1)/z][\alpha+1-(A\alpha+1)/z]+(A/z-A)A\alpha/z}\,Vb \qquad (A.I-10)$$

The condition of oscillation is given by

$$V_3/Vb = 1. \qquad (A.I-11)$$

From (A.I-5) and (A.I-9) to (A.I-11), we obtain

$$z^2[(1-2A+2A^2)+2(1-A)\alpha+\alpha^2]-2z[(1-2A+2A^2)+\alpha+A\alpha^2]$$

$+ [(1-2A+2A^2)+2A\alpha+2A^2\alpha^2]=0$ (A.I-12)

For the roots to occur on the unit circle in the z plane, the characteristic equation must take the form (Fig.A.I.2)

$$z^2-2\psi z + 1 = 0. \quad \text{(A.I-13)}$$

Equations (A.I-12) and (A.I-13) give

$$2(1-A)+\alpha = 2A+2\alpha A^2 \quad \text{(A.I-14)}$$

since $\psi = \cos wT$ then

$f_o = (fc/2\pi) \arccos \psi.$

9.2 APPENDIX II

A. Derivation of stray-insensitive Integrator Errors due to Amplifier Finite Gain and Finite Bandwidth and Nonzero Switch-on Resistances.

To carry out the analysis of the noninverting integrator, we assume an ideal two-phase clock with a 50 percent duty cycle. Note that the results obtained can also be applied to the inverting integrator, with the only difference that the corresponding output signal appears at the inverse phase (e.g., $m^-_{,2} = m^+_{,1}$ and vice versa).

9.2.0.1 Phase 1: $(n < t \leq n+1/2)$:

The integrator input signal Vi in Fig.A.II.1 is assumed to be constant during this phase. Combining the principle of charge conservation with Ohm's and Kirchhoff's laws, and neglecting all second- or higher order error terms, the time domain solutions can easily be derived. For t = tp(n+1/2), we obtain the following voltages:

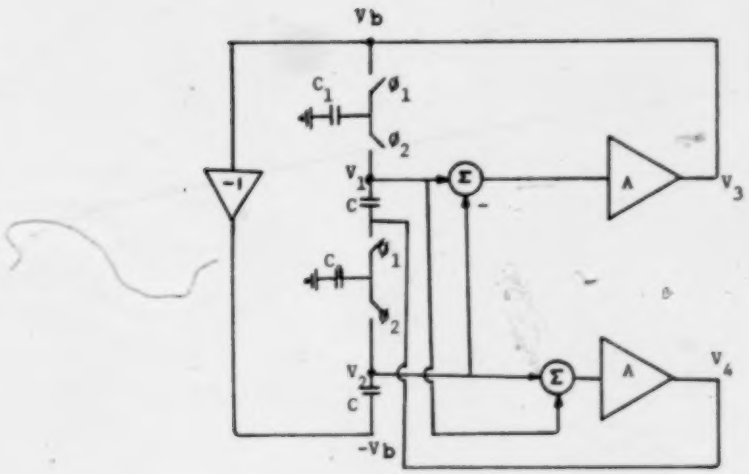


Fig. A.I.1 SCO using sequence discriminator.

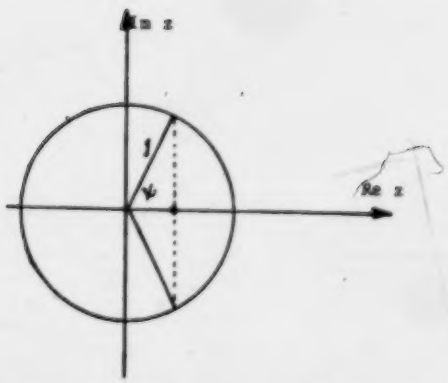


Fig. A.I.2Location of the characteristic polynomial roots in the z plane.

$$Vk_1(n+1/2) = Vi_1(n+1/2)[1+\epsilon k]$$

$$Vd_1(n+1/2) = Vo_1(n+1/2)-Vo_2(n)+Vd_2(n)$$

$$Vo_1(n+1/2) = Vo_2(n)[1-\epsilon A]-Vd_2(n)[1-\epsilon A-\epsilon B]$$

$$\epsilon k = \exp[-tc/tk] \qquad tk = 2Ron\ kC \qquad tc = tp/2$$

$$\epsilon B = \exp[-tc\ B] \qquad B = 2\pi fT$$

$$\epsilon A = 1/A_o$$

(A.II-1)

9.2.0.2 Phase 2: $(n+1/2 < t \leq n+1)$:

The corresponding circuit is shown in Fig.A.II.2. Instead of solving a system of first-order differential equations in the time domain, it is more convenient to transform the whole system into the Laplace domain, where we have to solve only a system of linear equations. The time domain solution is then obtained via the inverse Laplace transform.

The integrator network can be described by the following Laplace transform pair:

$$[\dot{V}d_2-\dot{V}o_2]-(1/t_o)[Vk_2-Vd_2] = 0 \qquad t_o = 2Ron\ C$$

$$\dot{V}k_2+(1/tk)[Vk_2-Vd_2] = 0 \qquad tk = 2Ron\ kC$$

$$\dot{V}o_2+(B/A_o)Vo_2+B\ Vd_2 = 0$$

(A.II-2a)

$$s[Vd_2-Vo_2]-[Vd_1(n+1/2)-Vo_1(n+1/2)]-(1/t_o)[Vk_2-Vd_2] = 0$$

$$sVk_2-Vk_1(n+1/2)+(1/tk)[Vk_2-Vd_2] = 0$$

$$sVo_2-Vo_1(n+1/2)+Vo_2(B/A_o)+BVd_2 = 0$$

The solution of this system of equations is rather tedious and, therefore, not given in detail here. After

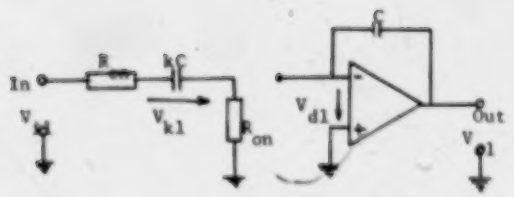


Fig. A.II.1 Noninverting nonideal SC integrator during phase 1.

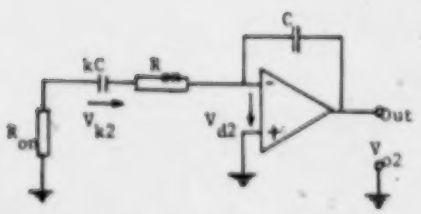


Fig. A.II.2 Noninverting nonideal SC integrator during phase 2.

some mathematical effort, we finally obtain the following solution for the two voltages Vd and V_o at the discrete time t = tp(n+1):

$$Vd_2(n+1) = (1/1+k)*$$

$$*[Vd_1(n+1/2)-Vo_1(n+1/2)+Vo_2(n+1/2)-kVi_1(n+1/2)[1-2\epsilon k]]$$

$$Vo_2(n+1) =$$

$$Vo_1(n+1/2)[R_{21}+\epsilon_1(R_{11}+R_{22})+\epsilon_2(R_{12}+R_{23})]-Vd_1(n+1/2)@$$

$$@\ [R_{21}+\epsilon_1 R_{22}+\epsilon_2 R_{23}]+Vk_1(n+1/2)kR_{12}[1+\epsilon_1 w_2 tk/D+\epsilon_2 w_1 tk/D]$$

(A.II-2b)

$$R_{11} = -(1/D)[1+k-w_1 tk]$$

$$R_{12} = (1/D)[1+k-w_2 tk]$$

$$R_{21} = (B/w_1\ w_2\ tk)R_{22} = (B/w_1 D)[1-w_1 tk]$$

$$R_{23} = -(B/w_2 D)[1-w_2 tk]$$

$$w_1 tk = (1/2)[1+k+Btk(1+\epsilon A)+D]$$

$$w_2 tk = (1/2)[1+k+Btk(1+\epsilon A)-D]$$

$$\epsilon_1 = \exp[-tc\ w_1]$$

$$\epsilon_2 = \exp[-tc\ w_2]$$

$$D^2 = [1+k-Btk(1+\epsilon A)]^2+4kBtk$$

Depending on whether we solve the system for $V_o(n+1)$ (switching phase 2 at the output) or $V_o(n+3/2)$ (switching phase 1 at the output), we eliminate the corresponding equations at t=tp(n+1/2) or t=tp(n+1), respectively. The resulting new system of equations contains only voltages, which are exactly one clock period apart in time, making it easy to apply the

Z-transform. Finally, we can eliminate the variable Vd(z) and solve for the transfer function. The two resulting transfer functions (for the two switching phases at the output) are

$$H_{11}(z) = k[z^{-1}/(1-z^{-1})]\, E_{11}(z)$$

$$E_{11}(z)=\{(1-z^{-1})/[1+k-z^{-1}(1+\alpha k)]\}*$$
$$*[(1+\beta k)(1-\epsilon A)-\epsilon B(1-\beta)-2\epsilon k]$$

$$H_{12}(z) = k[z^{-1/2}/(1-z^{-1})]E_{12}(z)$$

$$E_{12}(z) =$$
$$\{(1-z^{-1})/[1+k-z^{-1}\ (1+\alpha k)]\}\beta\{1+k+z^{-1}[(\alpha/\beta)(1-2\epsilon k)-1]\}$$

$$\alpha = R_{21}+\epsilon_1(R_{11}+R_{22}) +\epsilon_2(R_{12}+R_{23})$$

$$\beta = R_{21}[1-\epsilon k+\epsilon_1 w_2 tk/D - \epsilon_2 w_1 tk/D]$$

(A.II-3)

The corresponding magnitude and phase errors in the frequency domain are already given in (A.II-1). For the simplified case of ideal switches (Ron = 0) and provided that $\epsilon A \ll w\ tp$ holds, we obtain

$$m_{11}(w) = -\epsilon A(1+k/2)-\epsilon_2(k/1+k)$$

$$\theta_{11}(w) = \epsilon A[k/2\ \tan(wtp)] \qquad \text{(A.II-4)}$$

$$m_{12}(w) = -\epsilon A(1+k/2)-\epsilon_2[1-(\text{Cos } wtp)/(1+k)]$$

$$\theta_{12}(w) = \epsilon A[k/2\ \tan(wtp)]-\epsilon_2[(\text{Sin } wtp)/(1+k)]$$

$$\epsilon_2 = \exp[-tc\ w_2] \qquad w_2 = B[(1/(1+k))+\epsilon A]$$

B. Derivation of the Errors for Unity-Gain Amplifier Integrators

1. Errors due to nonzero switch-on resistances: To simplify the analysis procedure, we assume that the integrator input voltage remains constant during its

active phase (i.e., when it is applied to the network). Using the switch model given in Fig.3.5 and applying the principle of charge conservation, both circuits in Fig.3.6 can be discribed by the following, except the sign of the input voltage, identical charge equation:

$$\pm Vi_1(n+1/2)kC(1-\epsilon k)+Vo_2(n)C = Vo_2(n+1)\pm Vi_1(n+1/2)k\,C\,\epsilon k \qquad \text{(A.II-5)}$$

$\epsilon k = \exp(-tc/tk)$; $tc=tp/2$; $tk=2Ron\ kC$

By transforming (A.II-5) into the Z-domain and solving for the transfer function $Vo_2(z)/Vi_1(z)$, we obtain

$$H_{12}(z) = \pm k[z^{-1/2}/(1-z^{-1})](1-2\epsilon k) \qquad \text{(A.II-6)}$$

2. Errors due to stray-capacitances: Considering the stray-capacitances as the only circuit nonidealities, the charge equations, describing the two integrator circuits given in Fig.3.6, are slightly different. The corresponding equations for the two networks are

   a. noninverting integrator:

   $$Vn(n+1/2)C[k+\epsilon ks]+Vo_2(n)C[1+\epsilon s] = Vo_2(n+1)C[1+\epsilon s+\epsilon ks] \qquad \text{(A.II-7a)}$$

   b. inverting integrator:

   $$-Vn(n+1/2)kC+Vo_2(n)C[1+\epsilon s] = Vo_2(n+1)C[1+\epsilon s+\epsilon ks] \qquad \text{(A.II-7b)}$$

3. Using only first-order error terms, the nonideal Z-domain transfer functions are readily obtained as

a. noninverting integrator:

$$H^{+}_{12}(z) = [kz^{-1/2}(1+\epsilon ks/k)]/[(1+\epsilon s)(1+\epsilon ks-z^{-1})] \quad \text{(A.II-8a)}$$

b. inverting integrator:

$$H^{-}_{12}(z) = -[kz^{-1/2}/(1+\epsilon s)\ (1+\epsilon ks-z^{-1})] \quad \text{(A.II-8b)}$$

9.3 APPENDIX III

9.3.1 SCO applications

The oscillation frequency of the SCO is controlled by the clock repetition rate and the number of samples k in each sinusoidal oscillation cycle at the SCO output. k is independent of the clock. One very important application of such a device is in the area of frequency compression of frequency modulated (FM) signals. The reduction of the FM bandwidth of the received FM signal results in an improvement of detection threshold level. In addition, using SCO , the center frequency fcen of the FM signal; as well as the modulation index β, can be scaled down by a factor k. This allows the detection to be performed at lower frequencies, simplifying the design of the detector.

Existing approaches for FM threshold extention use the negative feedback demodulator or phase locked loop (PLL) demodulator. In both cases the feedback loops are employed where extra care is needed to satisfy the stability requirements.

In the proposed approach[44], the FM signal is converted into a pulse train with time-varying period. This pulse train is used as the clock controlling the switches of the SCO.

9.3.2 Frequency Compression using SCO

The SCO output, for a clock of equal periods, is a sampled and held sinusoidal wave. One of the SCO's is shown in Fig.4.12a. It has a fundamental frequency of oscillation given by:

$$f_o = (fc/\pi)\mathrm{Sin}^{-1}(C_1/2C) = fc/k \qquad \text{(A.III-1)}$$

Now, let us examine the response when the clock does not have equal repetition periods. As illustrated in Fig.AIII.1, the SCO output changes its amplitude in discrete manner from A cos(2nπ/k) to A cos(2(n+1)π/k) at the instant of clock state-transition, independent of the clock periods. In the light of this simple, but important, observation, the analog FM signal is hard limited. The resulting pulse train with time varying period is used as the clock controlling the switches in the SCO.

Refering to the block diagram in Fig.A.III.2, we can write the expression for the SCO output as

$$Vs(t) = A \sum_{-\infty}^{+\infty} p(\theta - 2n\pi)\mathrm{Cos}(2n\pi/k) \qquad \text{(A.III-2)}$$

where $\theta(t)$ = wcen t + $\psi(t)$ corresponds to the original FM signal Cos (wcen t + $\theta(t)$). p(t) is the rectangular function. We can rewrite (A.III-2) as

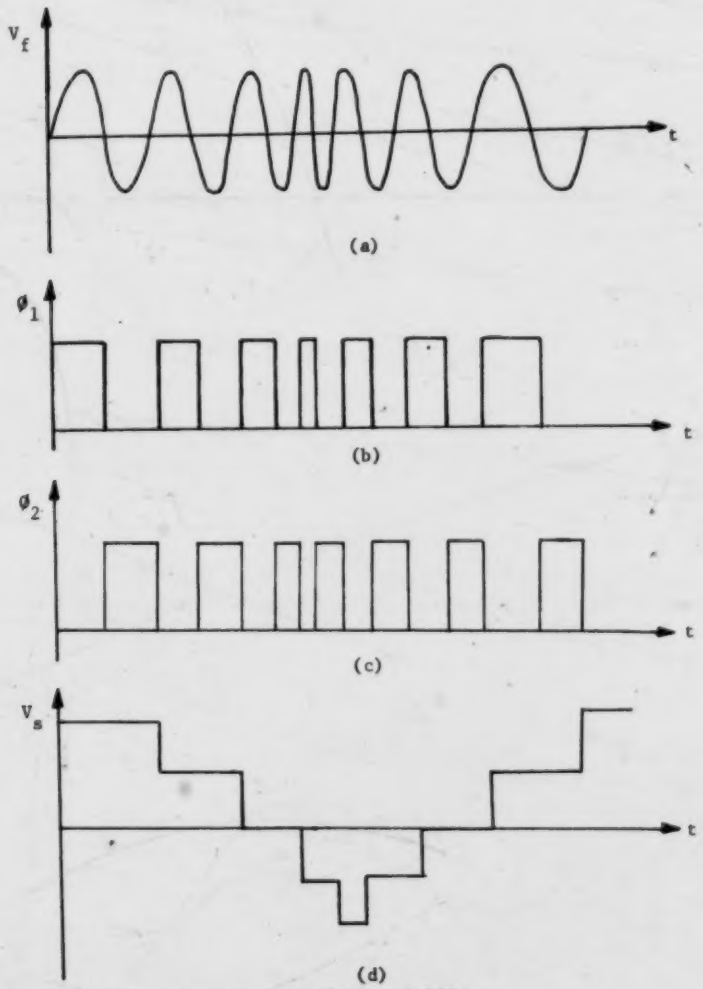
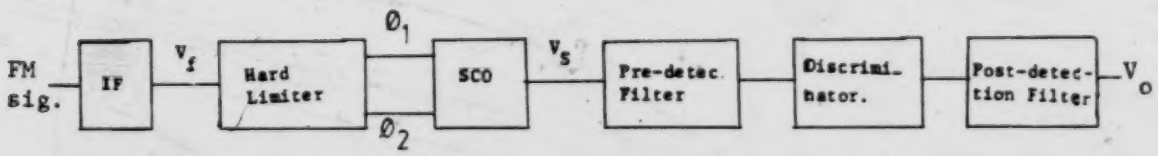


Fig. A.III-1 Input and output waveforms of SCO.
(a) Frequency modulated signal
(b) Clock ϕ_1
(c) Clock ϕ_2 and (d) SCO output (k=10).



Fig,A.III.2 Block diagram of proposed FM receiver.

$$Vs(t) = [Ap(\theta)][\sum_{-\infty}^{+\infty} \partial(\theta - 2n\pi)Cos(2n\pi/k)] \qquad (A.III-3)$$

$$= A[p(\theta)]\{Cos(1/k)\ [wcen\ t+\psi(t)]\ \sum_{-\infty}^{+\infty}\partial[\ wcen\ t+\psi(t)-2n\pi]\}$$

$$=A[p(\theta)]\{Cos(1/k)[wcen\ t+\psi(t)]1/2\pi[1+\sum_{-\infty}^{+\infty}2Cos(2nwcen\ t+n\psi(t))]\}$$

From (A.III-3) it is seen that Vs(t) contains the frequency component

$Cos((wcen\ t)/k + (1/k)\psi(t))$.

This is the original FM signal compressed in frequency by the factor k. According to (A.III-3) some constraints here to be imposed on the compression factor k. The lower limit of k should be chosen such that the unwanted spectra can be removed easily. Therefore k must be much greater than 1. Since the center frequency fcen is divided by the same factor k as the modulation index β, then the upper limit of k should be small enough so that fcen/k >> Bn (modulating signal Bandwidth). Since the center frequency of the analog FM signal can be easily shifted up or down by heterodying, then the condition, fcen/k >> Bn can be always met while still satisfying k >> 1. The reduction of the required detector BW implies a similar reduction in the detected uncorrelated noise BW. The net effect of frequency compression is reducing the detected noise power without affecting the signal power resulting in a SNR improvement of the compressed FM receiver. We can show that frequency compression can be accomplished without affecting the signal power.

The unique feature of translating center frequency down by the same factor k allows the detection to be designed at lower frequencies. This will enable using low frequency active devices to implement the discrimination. For instance, the active bandpass filter can function like a slope detector (or two active bandpass filters combined form a balanced slope detector).

9.4 APPENDIX IV

9.4.1 Sequence Discriminator Multiphase oscillators

In this section, the design of multiphase oscillators which is based on the active sequence discriminator (SD) is presented. An SD is an n-path symmetric network, (Fig.A.IV.1). Its operation is briefly explained here.

A sequence V1, V2, ... , Vn is defined as a set of signals which are equal in amplitude and equally spaced in phase. In exponential form, a sequence can be expressed as

$$Vi = V \exp(-j2\pi i/n),\ i=\pm1,\pm2,\ .\ .\ .\ ,\pm n. \qquad \text{(A.IV-1)}$$

A sequence is defined as a positive sequence if i is positive in (A.IV-1), or a negative sequence if i is negative. Practical asymmetric inputs to the SD can be applied which can be resolved into both positive and negative sequences. Let a positive sequence [Vin]p can be written as

$$[Vin]p = \begin{vmatrix} \exp(-j2\pi/n) \\ \vdots \\ \exp(-j2\pi(n-1)/n) \end{vmatrix} V \qquad \text{(A.IV-2)}$$

where V is the amplitude of each component of the input sequence.

It can be shown[43] that for the inputs given by (A.IV-2) the chain matrix for any path (k and ground as an input port, k' and ground as an output port, k=1,2, . . . ,n) is given by

$$\begin{vmatrix} Vk \\ Ik \end{vmatrix} = \frac{1}{p\ Y_1+Y_2\exp(2\pi j/n)} \begin{vmatrix} Y_1+Y_2 & 1 \\ Y_1Y_2[\ 2-\exp(2\pi j/n)-\exp(-2\pi j/n)] & Y_1+Y_2 \end{vmatrix} \begin{vmatrix} Vk' \\ -Ik \end{vmatrix} \qquad \text{(A.IV-3)}$$

The negative input sequence [Vin]n, and the chain matrix for any path can be written in the same form as (A.IV-2) and (A.IV-3), respectively by replacing j by -j.

The open-circuit voltage transfer function for the positive sequence Tp as obtained from (A.IV-3) is

$$Tp = [Vk'/Vk] \text{ at } p = [Y_1+Y_2\exp(2\pi j/n)]\ /(Y_1+Y_2) \qquad \text{(A.IV-4)}$$

The open circuit transfer function for the negative sequence Tn is given by replacing j by -j in (A.IV-4).

As a result of network symmetry, the outputs due to the positive input sequence can be expressed as

$$[V_o]p = \begin{vmatrix} \exp(-2\pi j/n) \\ \\ \exp(-2\pi j(n-1)/n) \\ 1 \end{vmatrix} V' \qquad \text{(A.IV-5)}$$

where V' is the amplitude of each component of the output sequence. Again, $[V_o]n$ is obtained from (A.IV-5) by substituting j by -j.

By examining the transfer functions Tp and Tn, it is seen as

$Y_1 = -Y_2 \exp(j2\pi/n)$ or $Y_1 = -Y_2 \exp(-j2\pi/n)$, one type of input sequence is nulled at a specific frequency f_o, leaving only the other at the output. As a consequence, the output signals at f_o form, ideally, a perfect sequence. Therefore the SD functions as a frequency-selective network. The remaining output sequence at f_o can be passed through an appropriate feedback network to the SD input in a regenerative manner to realize an oscillator at f_o, Fig.A.IV.2. The feedback network consists of summing and subtracting circuits and amplifiers from which the proper feedback signals can be derived.

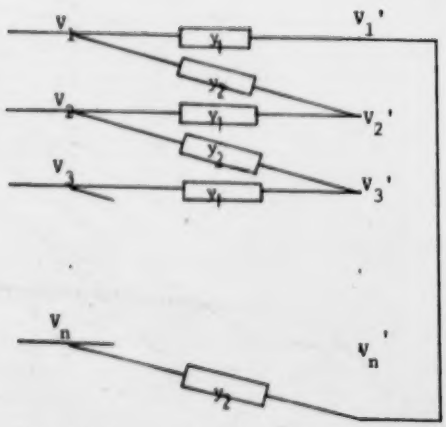


Fig.A.IV.1 Sequence discriminator.

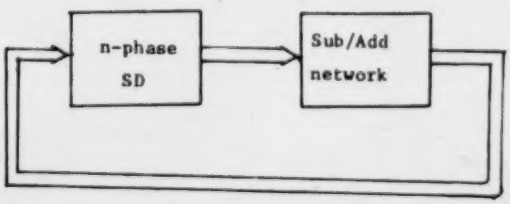


Fig.A.IV.2 Block diagram of SD oscillator. (The feedback network contains n-inputs, n-output ports summation/subtraction circuits.)